MODEL 8120

TIME CODE GENERATOR

OPERATION AND MAINTENANCE MANUAL

SERIAL NO B045

AUSTRON

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AUSTRON

AUSTRON INC. P.O. BOX 14766 - EXIT 248, N. IH 35, AUSTIN, TEXAS 78761 (512) 251-2341 TWX 910/874-1356

MODEL 8120

TIME CODE GENERATOR

OPERATION AND MAINTENANCE MANUAL

SERIAL NO B045

DECEMBER 1985

P/N 12708708

WARRANTY

AUSTRON, Inc. of Austin, Texas, warrants for one year after delivery to the original purchaser of any product manufactured by AUSTRON, that same shall be free of defects in material and workmanship. Obligation under this warranty shall be limited to repair or replacement, at AUSTRON's discretion, of any product or part thereof which has been returned by the original purchaser with transportation prepaid, and upon examination by AUSTRON, is found to be defective. AUSTRON assumes no responsibility for loss or damage to equipment being returned for repair or replacement under the terms of this warranty.

For this warranty to be effective, the purchaser agrees that the equipment will be properly installed and maintained. Equipment which, upon examination by AUSTRON, requires repair or replacement of parts thereof as a result of improper installation, misuse, unauthorized alterations or repairs, or user negligence, such repairs or replacement of parts thereof will be made at cost.

AUSTRON makes no representation or warranty of any kind, either expressed or implied, with respect to equipment operation and procedures. Any action that the user may take in reliance upon the operation or accuracy of this equipment shall be taken solely upon the user's own responsibility and risk.

AUSTRON shall not be liable for consequential damages to purchaser, user, or any others resulting from the possession or use of this equipment.

Prior to return of a product under terms of this warranty, AUSTRON, Inc., Austin, Texas, is to be notified. Notification is to include the model number and serial number of the product and full details of the problem.

INTRODUCTION

This manual is for personnel operating or maintaining the Model 8120 Time Code Generator manufactured by AUSTRON, Inc. It contains information concerning the physical and electrical specifications, installation, adjustment and operational procedures, and theoretical descriptions. In addition, the manual provides parts lists, assembly drawings, schematics and block diagrams.

AMENDMENT NOTICE

AUSTRON, Inc. makes every attempt to provide up-to-date manuals with the associated equipment. Occasionally, changes are made to the equipment wherein it is necessary to provide amendments to the manual. If any amendments are provided for this manual they are printed on paper stock other than white and will be found at the rear of this manual.

NOTE

The content of any amendments may affect operation, maintenance or calibration of the equipment.

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1. GENERAL DESCRIPTION

1.1. SCOPE OF SECTION

Section One introduces the AUSTRON Model 8120 Time Code Generator. Provided here is the description of the equipment including variations and options. Also, there is a brief discussion of the unit's input/output signals as well as environment, power, and packaging requirements.

1.2. PURPOSE OF EQUIPMENT

The Model 8120 Time Code Generator is a precise digital clock which generates a serial time code. It is a highly flexible unit which may be used in many applications where real or elapsed time must be maintained for control, recording or display. The serial time code may be used for central timing applications, or for recording continuous time on magnetic tape.

The basic unit accumulates, displays and outputs time in hours, minutes and seconds. The full count is 23 hr: 59 min: 59 sec. Reset is to 00:00:00. Preset thumb wheel switches are provided for entering initial time in hours through seconds. The serial code format is modified IRIG B (BCD hours, minutes and seconds) in both modulated (1 kHz carrier) and dc level shift form.

The basic unit is supplied with buffered, parallel, BCD outputs representing the accumulated time (hours through seconds) plus four simultaneous pulse rates. The BCD outputs may be expanded to include Days/ID and/or Milliseconds as options. The Days/ID option includes display, preset thumb wheel switches and related control for the three added digits. Days/ID is also added to the serial time code.

1.3. MODEL 8120 VARIATIONS

The Model 8120 can be modified to generate any of the standard IRIG (Figure 1-1, sheets 1, 2 and 3) NASA (Figure 1-2) or XR3 (Figure 1-3) code formats in place of, or in addition to, IRIG B (Figure 1-4, sheets 1 and 2), illustrate Slow Code, Types A and B, respectively. High stability oscillator, automatic start and WWV synchronization options are also available. An external time base input is standard on all units.

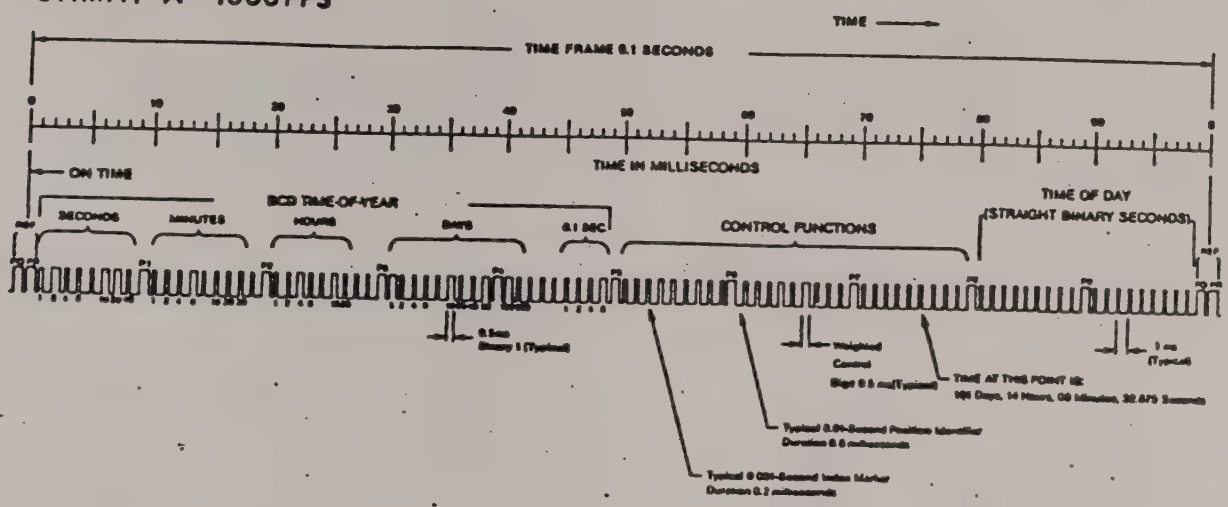
A large number of variations and extensions of this basic configuration are available as options. Refer to Table 1-1 for options available. Circuit descriptions for these options, when included, are provided in Chapter Six. Special modifications, when included, are described in Chapter Seven.

Table. 1-1: Standard Options.

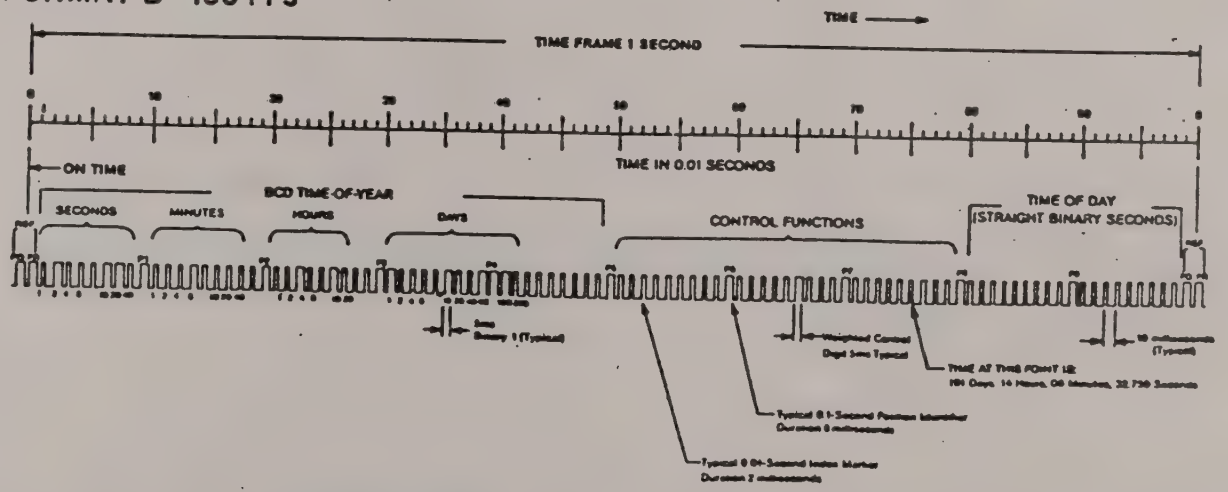
Option	Description
A12A	Slow Code, Type A
A12B	Slow Code, Type B
A16	Control Bit Insertion
A21	Computer Read Command/Data Freeze
B11	Crystal Oscillator (±1 part in 10 -9)
B13	Crystal Oscillator (±4 parts in 10 -9)
B14	Crystal Oscillator, Zero Warmup (±5 parts in 10 -7)
C11	Modified IRIG A (10 kHz) Code
C12A	Binary Seconds (17 Bits in Code)
C17	NASA 28-Bit (100 Hz) Code
C18	NASA 36-Bit (1 kHz) Code
C26	XR3 (250 Hz) Code
C26A	XR3 (1 kHz) Code
C31	IRIG G (100 kHz) Code
C41	IRIG A, B, Switch Selectable
C47	XR3 (250 Hz/1 kHZ) Switch Selectable
C48	IRIG H (100 Hz)
C48A	IRIG H (1 kHz)
C49	IRIG A, B, E, H, E (1 kHz), H (1 kHz), Switch Selectable
D14	Group Parallel BCD Outputs with Storage
E13	Days/ID Number
E14	Parallel BCD Output, Milliseconds
L12	48 Hz to 440 Hz Operation
L13	AC/DC Power Supply

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
—	RELEASED	11-18-85	OL

FORMAT A 1000 PPS

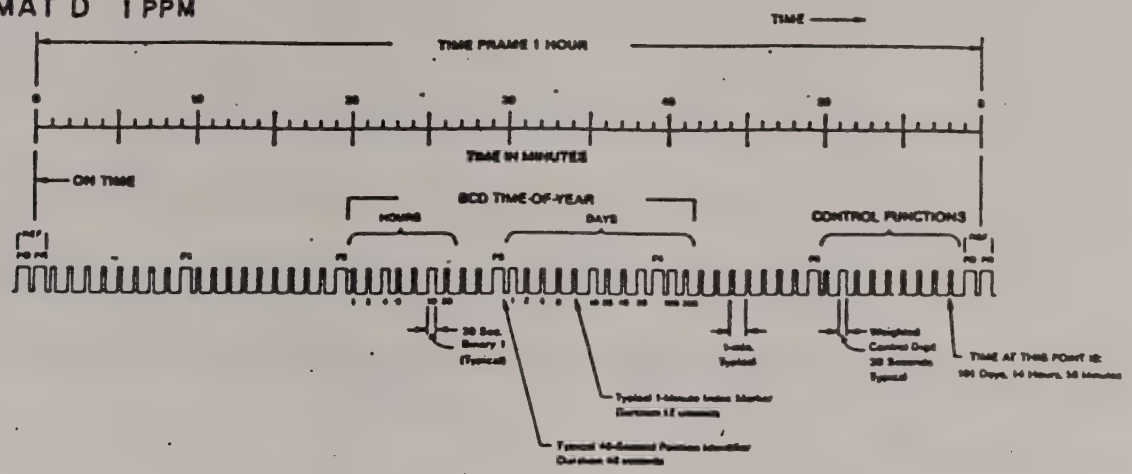


FORMAT B 100 PPS



		TOLERANCES UNLESS OTHERWISE SPECIFIED			AUSTRON INC. AUSTIN, TEXAS	
		DEC	FRAC	ANG		
		MATERIAL: —			IRIG TIME CODE FORMATS	
		Figure 1-1				
	8100	Q.A.			SIZE 1	CODE IDENT NO. 24672
NEXT ASSY	USED ON	ENGR			12408762	REV —
		CHECK	C Myles	11-18-85		
APPLICATION		DRAWN	P. JOHNSTON	11/18/85	SCALE NONE	SHEET 1 OF 3

FORMAT D 1 PPM



FORMAT E 10 PPS

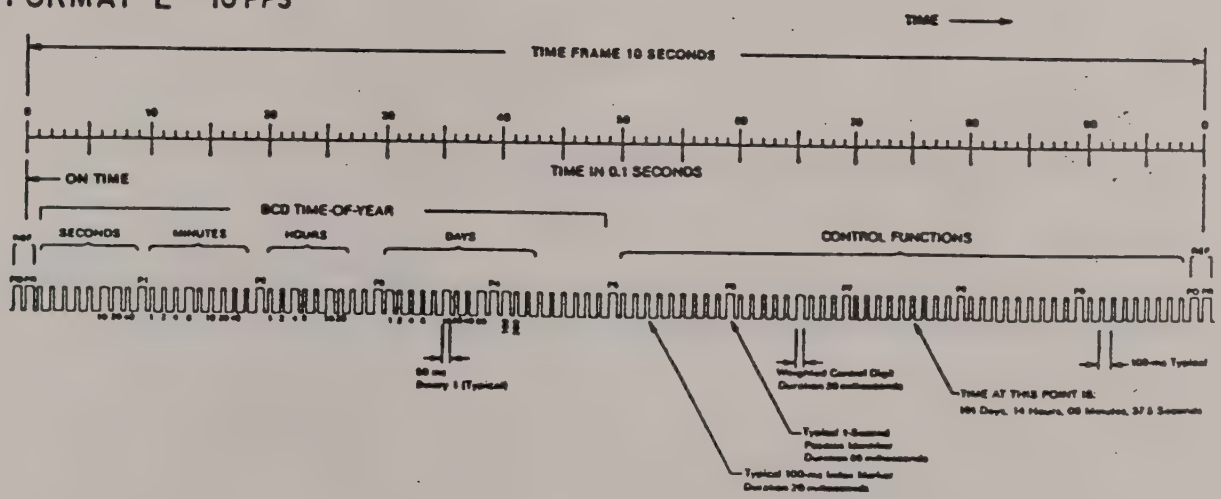
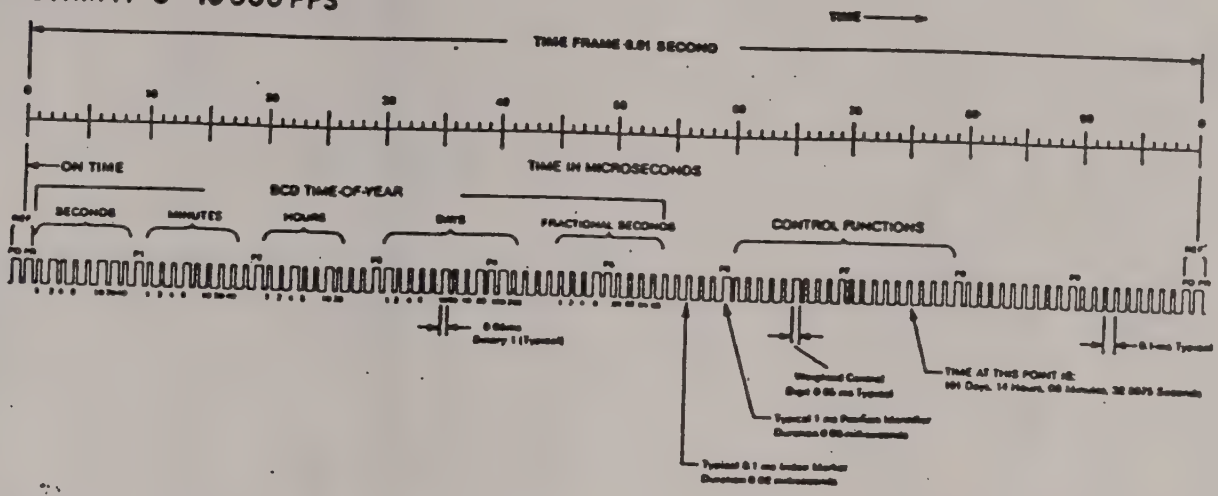


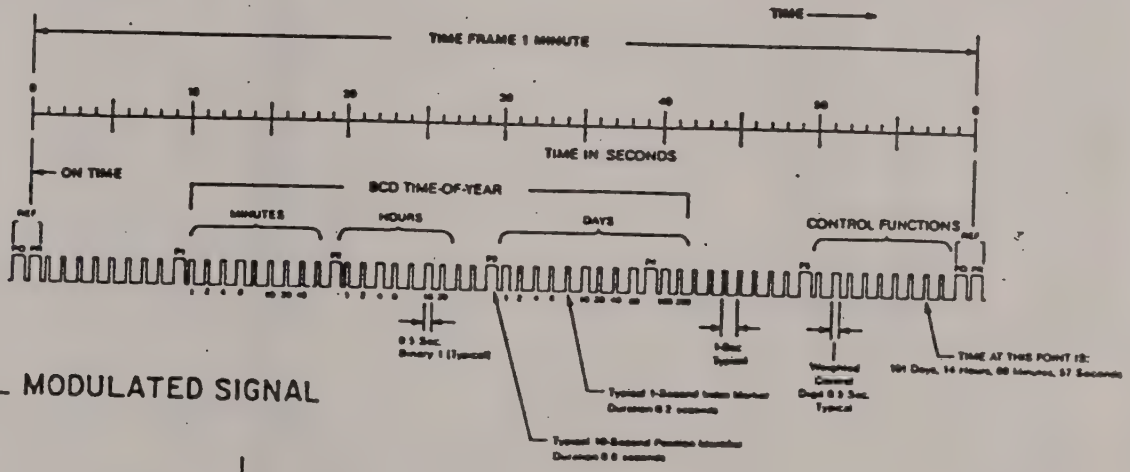
Figure 1-1

SIZE	CODE IDENT NO.		
1	24672	12408762	–
SCALE NONE		SHEET 2 OF 3	

FORMAT G 10000 PPS



FORMAT H 1 PPS



TYPICAL MODULATED SIGNAL

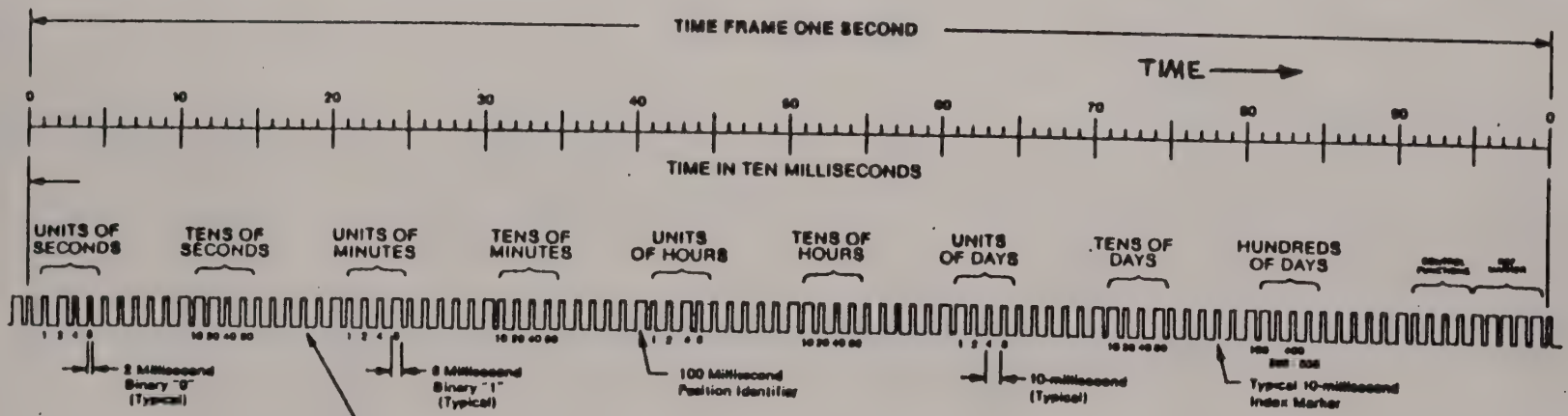
12408762

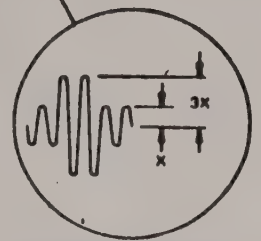
Figure 1-1

SIZE	CODE IDENT NO.		
1	24672	12408762	—
SCALE NONE		SHEET 3 OF 3	

NASA 36 BIT 100 PPS

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
	RELEASED	11-15-85	CRL





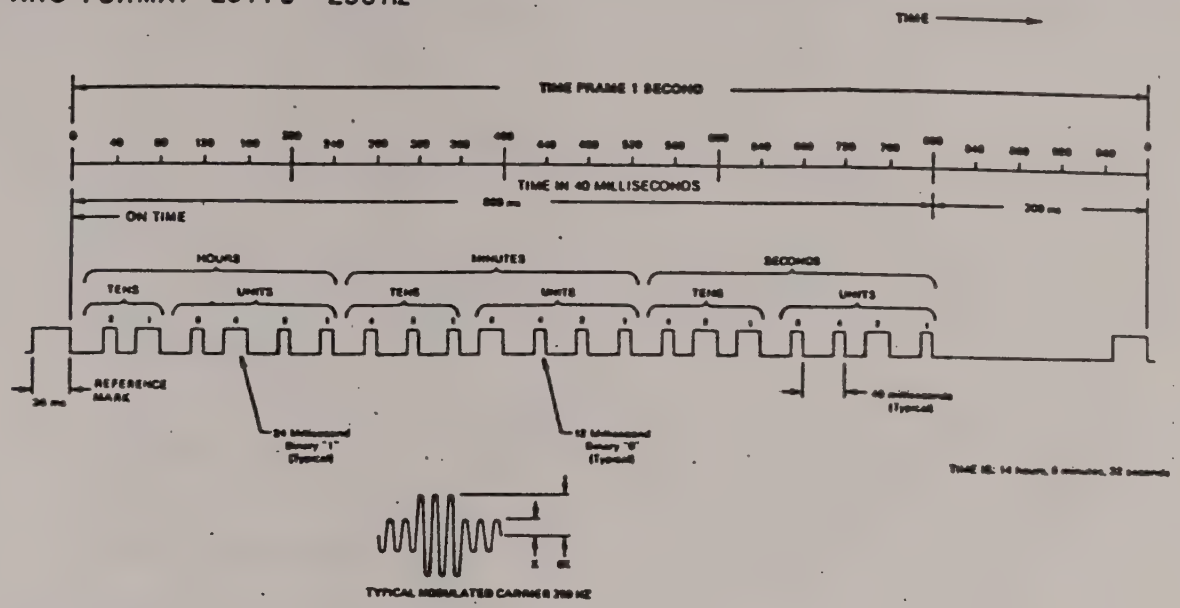
TYPICAL MODULATED CARRIER
CARRIER FREQUENCY 1000 HZ

1-6

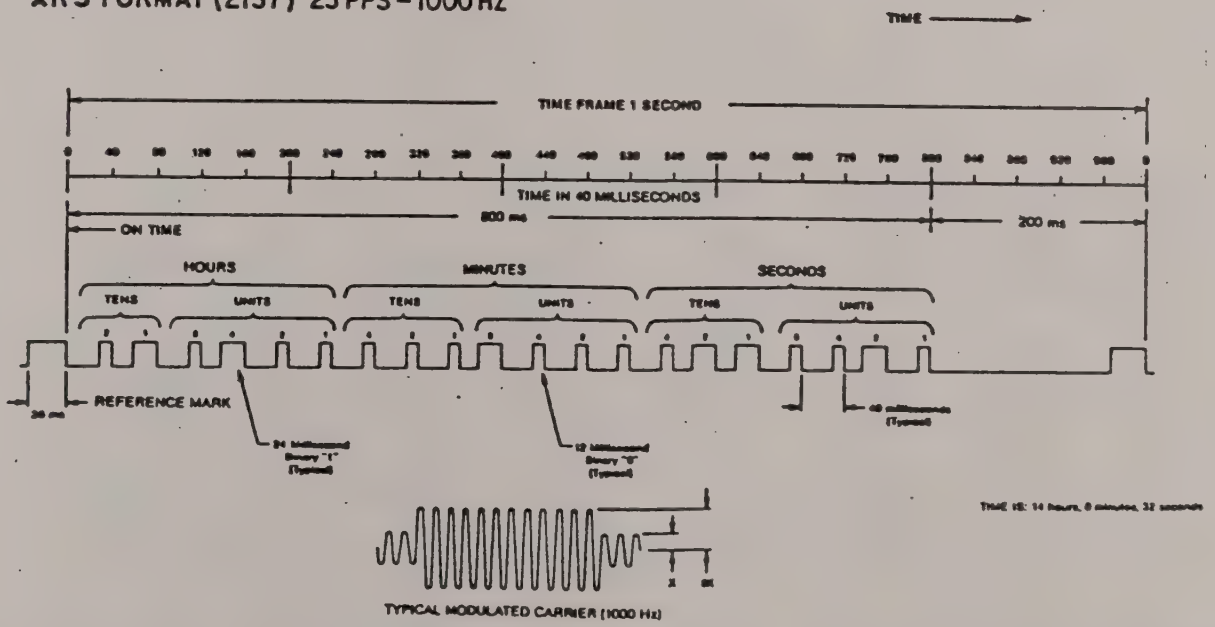
				TOLERANCES UNLESS OTHERWISE SPECIFIED	AUSTRON INC. AUSTIN, TEXAS
				DEC / FRAC / ANG	
				MATERIAL: Figure 1-2	NASA TIME CODE FORMAT
	8100			ENGR	SIZE 1 / CODE IDENT NO. 24672 / 12408763 / REV —
NEXT ASSY	USED ON	REF DES	FIG NO.	CHECK [illegible] 11-15-85	
APPLICATION				DRAWN P. JOHNSON 11-15-85	SCALE NONE / SHEET / OF

REVISIONS			
LTR	DESCRIPTION	DATE	APP.
—	RELEASED	11-18-85	DK

XR3 FORMAT 25 PPS – 250 HZ



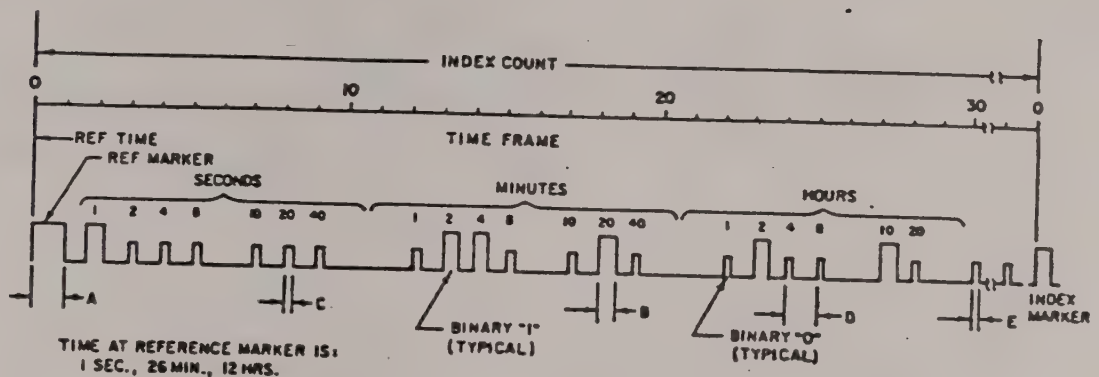
XR3 FORMAT (2137) 25 PPS – 1000 HZ



		TOLERANCES UNLESS OTHERWISE SPECIFIED			AUSTRON INC. AUSTIN, TEXAS		
		DEC	FRAC	ANG			
		MATERIAL: Figure 1-3			XR3 TIME CODE FORMATS		
	8100	Q.A.			SIZE 1	CODE IDENT NO. 24672	12408764 REV —
NEXT ASSY	USED ON	ENGR					
		CHECK	[illegible]	11-18-85			
APPLICATION		DRAWN	R. JOHNSON	11/18/85	SCALE NONE	SHEET 1 OF 1	

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
	RELEASED	11-15-85	CRL

TYPE A



	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs	1 Sec	1 Sec	500 ms	200 ms	200 ms	30
5	1/2 pps	60 Secs	2 Secs	2 Secs	1 Sec	400 ms	400 ms	30
6	1/10 pps	5 Mins	10 Secs	10 Secs	5 Secs	2 Secs	2 Secs	30
7	1/20 pps	10 Mins	20 Secs	20 Secs	10 Secs	4 Secs	4 Secs	30
8	1 ppm	30 Mins	1 Min	1 Min	30 Secs	12 Secs	12 Secs	30
9	1/2 ppm	60 Mins	2 Mins	2 Mins	1 Min	24 Secs	24 Secs	30

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DEC | FRAC | ANG

MATERIAL:
Figure 1-4

AUSTRON INC.
AUSTIN, TEXAS

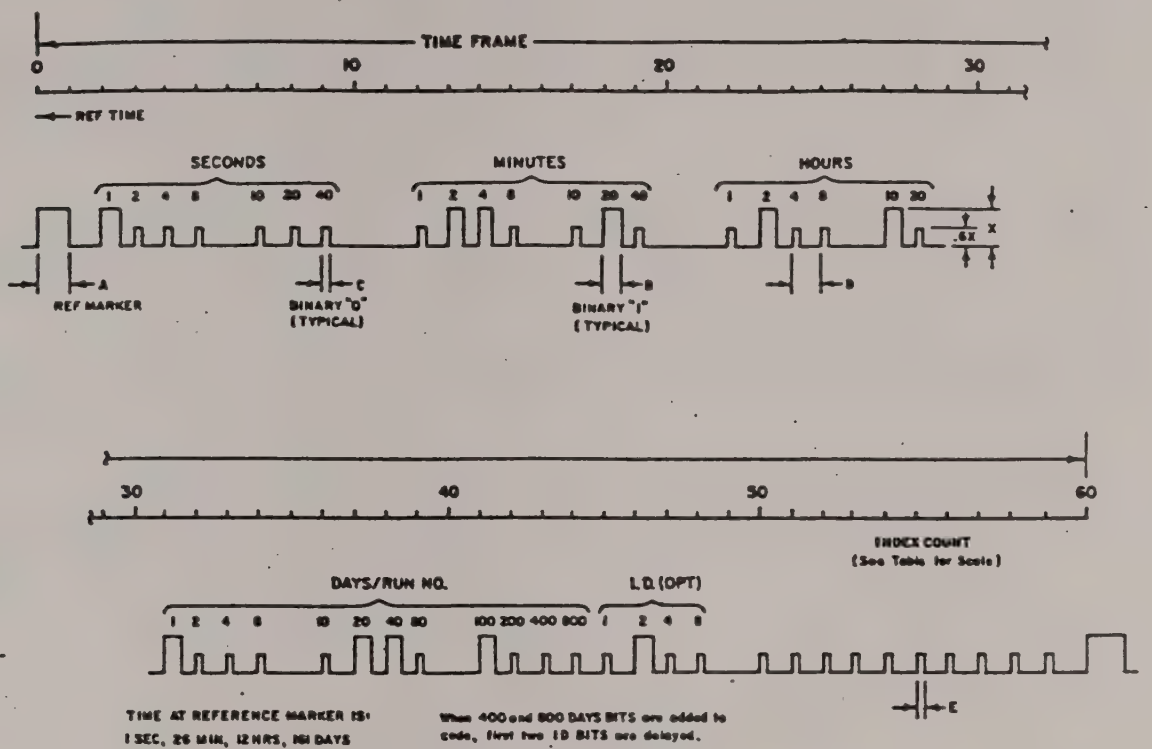
SLOW CODE
TYPE A & B

NEXT ASSY	USED ON				
	8100	Q.A.			
		ENGR			
		CHECK	[illegible]	11-15-85	
APPLICATION		DRAWN	P. JOHNSON	11-15-85	

SIZE	CODE IDENT NO.		REV
1	24672	12408765	—

SCALE NONE | SHEET 1 OF 2

TYPE B



	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	2 pps	30 Secs	1/2 Sec	1/2 Sec	250 ms	100 ms	100 ms	60
5	1 pps	60 Secs	1 Sec	1 Sec	1/2 Sec	200 ms	200 ms	60
6	1/2 pps	5 Mins	5 Secs	5 Secs	2 1/2 Secs	1 Sec	1 Sec	60
7	1/10 pps	10 Mins	10 Secs	10 Secs	5 Secs	2 Secs	2 Secs	60
8	2 ppm	30 Mins	30 Secs	30 Secs	10 Secs	6 Secs	6 Secs	60
9	1 ppm	60 Mins	60 Secs	60 Secs	30 Secs	12 Secs	12 Secs	60

Figure 1-4

SIZE	CODE IDENT NO.		
1	24672	12408765	—
SCALE		SHEET 2 OF 2	

1.4. SPECIFICATIONS

1.4.1. Time Base

The time base is a crystal-controlled oscillator with an aging rate of 1 part in 10 to the -7 per day and an over-all stability of 1 part in 10 to the -5 per day from 0°C to 60°C. Provision is included for the use of an external 1 MHz time base.

1.4.2. Input Signals

External Time Base: Accepts a 1 MHz input at 1 Vp-p (nominal) into 1 kilohm, via a rear panel BNC type connector. A rear panel switch selects INTernal or EXTernal time base.

Update Inhibit: A 5 Vdc level (or open circuit) enables update. A ground condition delays time update. Update may be delayed up to 0.8 s without losing a count via rear panel connectors, J3,46 or J4,13.

Elapsed Time: A 5 Vdc level (or open circuit) enables the unit to run. A ground condition stops the time base and deactivates the unit; pulse rates and code out are turned off. This input is on the rear panel J4,6.

1.4.3. Output Signals

NOTE

All output circuits are short-circuit-proof to ground.

Modulated Code: The modulated code is generated on a 1 kHz carrier with an adjustable amplitude from 0 Vdc to 10 Vp-p from a low impedance 15 mA source and adjustable modulation ratio (MARK-to-SPACE) from 2:1 to 6:1. Connector is rear panel BNC type. The Code Format is modified IRIG B with BCD hours, minutes and seconds.

DC Level Shift Code: The dc level shift code is generated with an adjustable amplitude from 0 Vdc to 10 Vdc into a minimum 600 ohm load. Connector is rear panel BNC type.

Parallel BCD Outputs: Updated time is provided as twenty-four parallel BCD bits (20 active) with leading edge on time. Levels are 0 Vdc to 5 Vdc (nominal) from a 6 kilohm source (DTL). The connector is at the rear panel, Amphenol 57-4036.

Code: 8-4-2-1

Logic: ONE = 5 Vdc $\pm$0.5 Vdc, behind 6 kilohm source
ZERO = 0 $\pm$0.5 Vdc, 12 mA sink

1.4.4. Display

A six-digit, in-line, in-plane display indicates time of day in hours, minutes and seconds. The Days/ID option adds three-digits. Numeral height is 0.55 in (14 mm).

1.4.5. Environmental Requirements

The operating and storage conditions recommended for the Model 8120 are below.

Operating: 0°C to 60°C at up to 95 percent relative humidity

Storage: -55°C to 85°C

1.4.6. Power Requirements

The unit uses 115/230 Vac ±10 percent, 48 Hz to 62 Hz at less than 30 watts. 48 Hz to 440 Hz operation is optional.

1.4.7. Physical Requirements

The Model 8120 is 3.5 in (89 mm) high by 19 in (483 mm) wide by 17 in (432 mm) deep. The unit has removable rack flanges and the chassis is drilled for Jonathan 120 QD series slides. The unit weight is approximately 23 lbs (10.4 kg) net; 35 lbs (16 kg) shipping.

2. INSTALLATION

2.1. SCOPE OF SECTION

Section Two describes the steps required to prepare the Model 8120 for operation and reshipment to another location. Included in this section are instructions for unpacking, inspecting, installing and storing the unit.

2.2. UNPACKING AND INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found, refer to the warranty at the front of this manual and to Section 2.5 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your AUSTRON representative.

2.3. CABINET MOUNTING

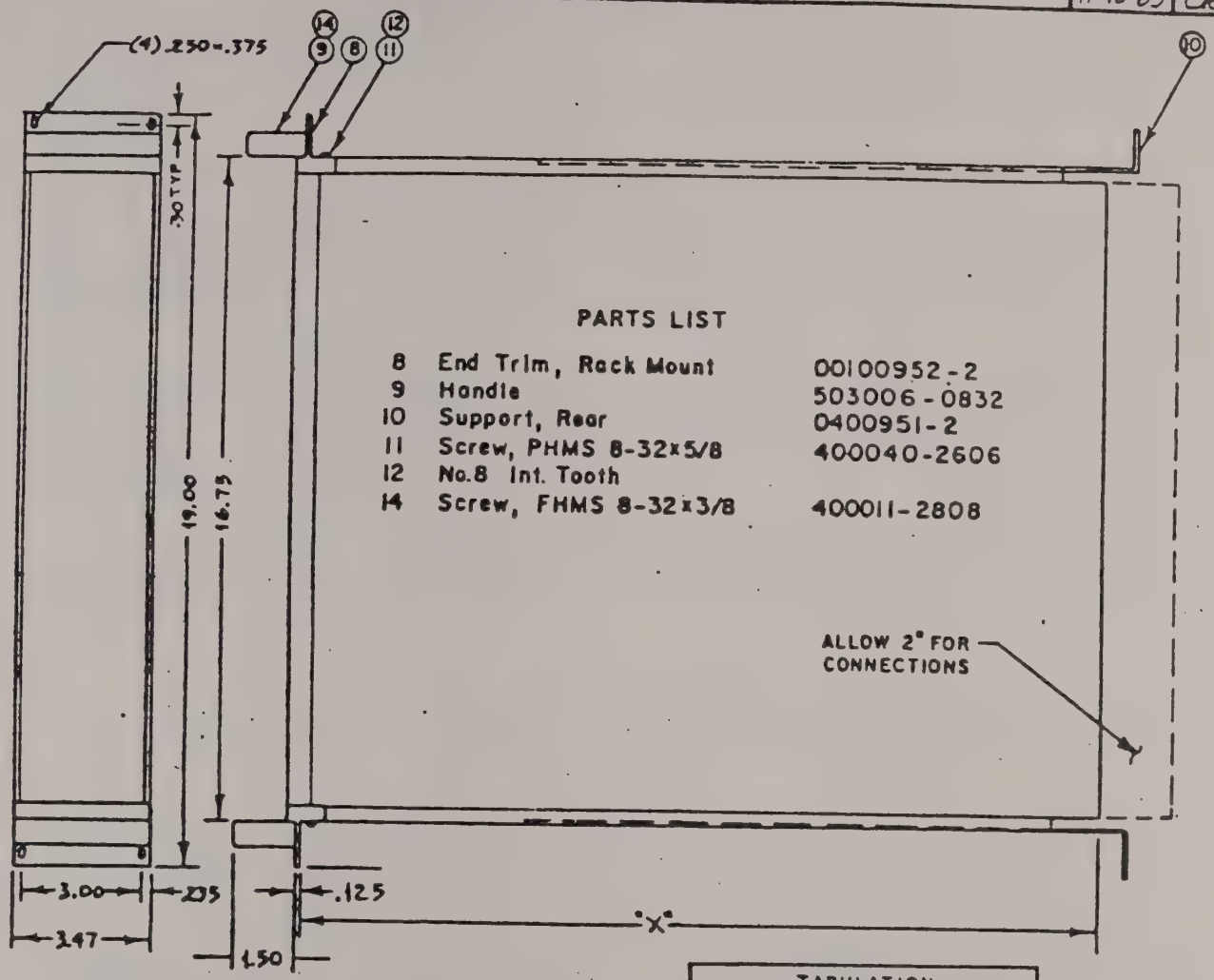
The standard Model 8120 is supplied with hardware for cabinet (rack-mount) installation as shown in Figure 2-1.

Refer to paragraph 1.4.7 for physical description and mounting requirements of the Model 8120.

WARNING

Do not obstruct the air flow through the outlet hole in the rear of the unit.

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
	RELEASED	11-15-85	CRL



PARTS LIST

8	End Trim, Rack Mount	00100952-2
9	Handle	503006-0832
10	Support, Rear	0400951-2
11	Screw, PHMS 8-32x5/8	400040-2606
12	No.8 Int. Tooth	
14	Screw, FHMS 8-32x3/8	400011-2808

NOTES:

1. Instr. are drilled to accept 20" Jonathan 120 QD series slides.
2. Item 10 deleted when shipped w/slides.

TABULATION		
P/L No.	"X"	Inst. Depth
39986-1	8.75	9.12
39986-2	10.75	11.12
39986-3	12.75	13.12
39986-4	14.75	15.12
39986-5	16.75	17.12
39986-6	18.75	19.12
39986-7	20.75	21.12

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DEC | FRAC | ANG

MATERIAL:
Figure 2-1

AUSTRON INC.
AUSTIN, TEXAS

3.5 IN (8.9mm) FULL RACK ASSEMBLY

NEXT ASSY	USED ON
	8100
APPLICATION	

Q.A.		
ENGR		
CHECK	[illegible]	11-15-85
DRAWN	P. Johnson	11-15-85

SIZE	CODE IDENT NO.		REV
1	24672	12408759	—

SCALE NONE SHEET 1 OF 1

2.4. INITIAL SETUP AND ADJUSTMENT

The EXT-INT switch on the rear panel must be in INT position to utilize the internal 1 MHz oscillator. If an external 1 MHz source is used, the switch must be in the EXT position.

Modulated Code (J9) Amplitude Adjustment Control on the Modulator PCB (a 100 kilohm potentiometer) must be adjusted to the input voltage required by the particular tape transport in use (1 Vp-p is standard for typical tape recorder). Voltage may be observed at CODE OUT JACK or at the MOD test point on the Modulator PCB. The voltage is factory set at 3 Vp-p.

The Modulation Ratio Control (a 5 ohm potentiometer) has been factory adjusted for 3:1 modulation ratio and should not require further adjustment. If adjustment should become necessary, the ratio control on the Modulation PCB may be adjusted as desired.

If the Level Shift output is also to be used, a dc potentiometer on the Modulator PCB may be adjusted for the desired output level. The range is 0 Vdc to 10 Vdc and is factory set at 6 Vp-p.

2.4.1. Rear Panel Controls and Connectors

Rear panel controls and connectors are described in Table 3-2. Refer to the table for hook up information.

2.4.2. Power Up

The Model 8120, unless otherwise specified, is supplied to operate from a 115 Vac $\pm$10 percent, 48 Hz to 62 Hz source.

To adapt the Model 8120, for 230 Vac operation, slide the rear panel 115/230 Vac selector switch, S101, to the 230 position and change fuse, F1, from 2 A slow-blow to 1A slow-blow.

To apply primary power to the Model 8120, turn the four-position mode switch to PWR OFF, install the power cord (supplied), and turn the switch to GENerate.

2.5. STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the original factory packaging, or use the best packaging methods available. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

2. If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb per sq in bursting strength) or wooden box to house the instrument.

3. Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

4. Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".

5. If shipping the unit to AUSTRON, refer to the warranty at the front of this manual and check with your AUSTRON representative for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

3. OPERATION

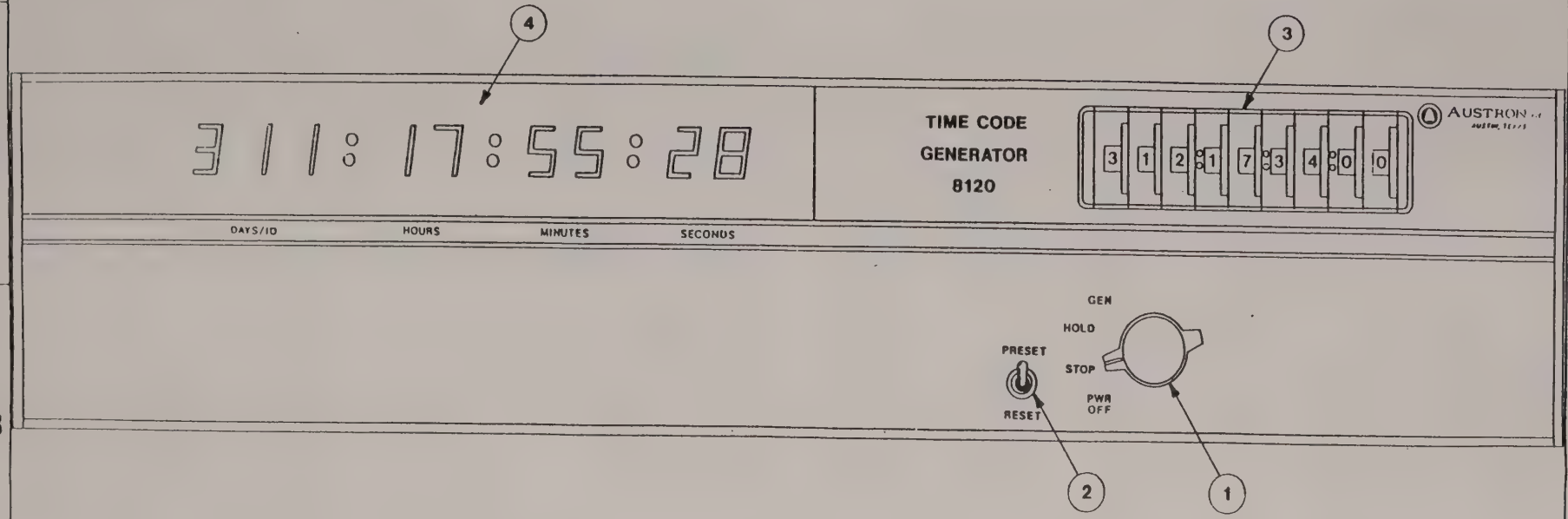
3.1. SCOPE OF SECTION

Section Three details controls, indicators, and connectors as to the operation of the Model 8120. It is advisable that the following description on use of the instrument controls and indicators be read before operating the unit.

Refer to Table 3-1 for a description of Front Panel Controls and Indicators and Drawing No. 12110183 for the illustration.

Refer to Table 3-2 and Drawing No. 12110184 for Rear Panel Controls and Connectors.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APP'D
	—	RELEASED	12-5-85	C.E.L.



3-2

TOLERANCES UNLESS OTHERWISE SPECIFIED		
DEC	FRAC	ANG
MATERIAL:		

AUSTRON INC.
AUSTIN, TEXAS

FRONT PANEL CONTROLS & INDICATORS, MODEL 8120

NEXT ASSY	USED ON	REF DES	FIG NO.
			3-1

APPLICATION

ENGR		12/3/85
CHECK		12-5-85
DRAWN		12/3/85

SIZE	CODE IDENT NO.		REV
2	24672	1211018 3	—

SCALE NONE | SHEET 1 OF 1

3.2. FRONT PANEL CONTROLS AND INDICATORS

The following table describes the Model 8120 front panel controls and indicators.

Table. 3-1: Front Panel Controls and Indicators.

	Device	Function
1.	Mode Selector (Rotary Switch, S3)	Controls main power and selects mode of operation.
	PWR OFF	Removes power to the unit.
	STOP	Arms PRESET/RESET switch. Stops time base counters. No outputs generated.
	HOLD	Stops the count in the display register. Latest count is displayed. Arms PRESET/RESET switch.
	GENerate	Permits normal update of the display register and generation of the serial time code.

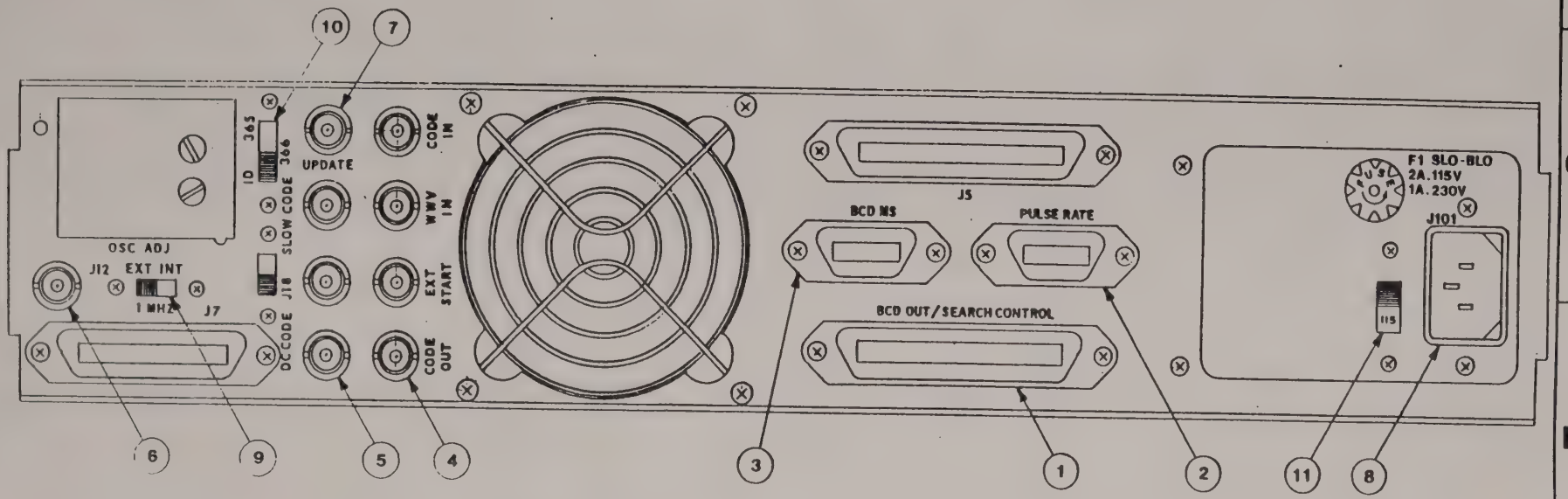
NOTE

When the mode selection switch is moved from STOP to HOLD, the code generation remains inhibited. When moved from GENerate to HOLD, code generation is normal, except that each frame will contain the same item information, since update does not take place in HOLD.

Table 3-1. Front Panel Controls and Indicators (Continued).

	Device	Function
2.	PRESET/RESET (Momentary Toggle Switch, S4)	In PRESET, loads contents of Preset thumbwheel switches into display register. In RESET, forces display register contents to zero. Preset and Reset to the six-digits of TOD is inhibited when the Mode Selector is in GEN to allow changing Days/ID (when so equipped) without disturbing the TOD.
3.	PRESET (Thumbwheel Switches: S6-11 for TOD, S12-14 for Days/ID)	Used to store start time for entry into the display register by PRESET/RESET switch.
4.	DISPLAY	A six-digit, in-line planar read-out which indicates TOD in hours, minutes and seconds. Days/ID Option adds three-digits.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	—	RELEASED	12-5-85	CPL



				TOLERANCES UNLESS OTHERWISE SPECIFIED			AUSTRON INC. AUSTIN, TEXAS
				DEC	FRAC	ANG	REAR PANEL CONTROLS & CONNECTORS, MODEL 8120
				MATERIAL:			
							SIZE 2 | CODE IDENT NO. 24672 | 12110184 | REV —
NEXT ASSY	USED ON	REF DES	FIG NO. 3-2	APPLICATION			SCALE NONE | SHEET 1 OF 1

3.3. REAR PANEL CONTROLS AND CONNECTORS

The following table describes the Model 8120 rear panel controls and connectors.

Table. 3-2: Rear Panel Controls and Connectors.

	Device	Function
1.	BCD OUT (50-pin connector, J3)	BCD output of display register contents.
2.	PULSE RATE (14-pin connector, J4)	Pulse rate and control lines.
3.	BCD MS, Optional (14-pin connector, J6)	BCD milliseconds outputs.
4.	CODE OUT (BNC connector, J9)	Modulated serial time code output.
5.	DC CODE (BNC connector, J10)	Serial level shift time code output.
6.	EXT 1 MHz (BNC connector, J12)	External 1 MHz Time Base input.
7.	ID UPDATE, Optional (BNC connector, J13)	ID UPDATE input (part of Days/ID option).
8.	AC POWER (AC connector, J101)	Mates with ac line cord.
9.	EXT/INT 1 MHz (Slide Switch, S1)	Selects external or internal 1 MHz Time Base.
10.	365-366 ID, Optional (Slide Switch, S16)	Leap Year/ID select switch (part of Days/ID option).
11.	115/230 V Power Select (Slide Switch, S101)	Adapts power transformer for 115 Vac or 230 Vac operation.

4. MAINTENANCE AND CALIBRATION

4.1. SCOPE OF SECTION

Section Four covers recommended maintenance and repair test equipment and procedures for the Model 8120. Instructions are included for calibration of the time code reader.

4.2. FACTORY SERVICE

When your Model 8120 requires service that cannot be accomplished on site, contact your AUSTRON representative. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your sales representative:

AUSTRON, Inc.
P. O. Box 14766
Exit 248 N. IH 35
Austin, Texas 78761

Specify both model and complete serial number in all correspondence. If necessary, you may phone AUSTRON at (Area Code 512) 251-2341.

4.3. ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five-to-six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1. Disconnect ac power and remove the top and bottom covers.

2. Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

3. Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a PCB contains IC packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4. Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5. If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean printed circuit boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. Do not use a high-powered vacuum cleaner device on small internal components.

6. Wipe the external surfaces of the instrument with a soft, damp cloth to remove dirt, fingerprints, and other foreign materials.

7. Replace the top and bottom covers and reconnect ac power. Perform the Operational Test and Calibration Procedure (Paragraph 4.4). If performance does not match or exceed the specifications listed in Section One of this manual, corrective maintenance is in order.

4.4. OPERATIONAL TEST AND CALIBRATION PROCEDURE

The Model 8120 is ready to operate immediately after turning on the power. Preliminary adjustments are not normally required.

Front panel controls and indicators are described in Table 3-1.

In the event of an equipment malfunction, the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the technician to isolate the trouble to a particular circuit board or subsection.

When the trouble is isolated, the functional description in Chapter Five and option information in Chapter Six will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply of this equipment. Use caution at all times when the protective covers are removed.

4.4.1. Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8120.

Table. 4-1: Test Equipment for Model 8120.

Model	Manufacturer	Description
546	Tektronix	Oscilloscope 50 MHz bandwidth triggered sweeps from 0.1 us/ cm to 5 s/cm.
6012	Tektronix	Probe, 10:1 attenuation ratio, 17 pF capacitance.
7003	Systron-Donner	DMM, 10 megohm input impedance, ±0.1 percent accuracy.

4.4.2. Power Supply
(Schematic Dwg. No. 12304810-09)

The following voltage checks will ensure the correct operation of the power supply, assuming a normal voltage of 115 Vac. The test points are available on the unit PCB edge connector, XA101. Refer to paragraph 5.3.7.3 for Power Supply Calibration.

4.4.2.1. Power Supply Calibration Procedure

Test Equipment: see Section Four, Table 4-1.

Check that fuse F1 is the proper size for the input voltage selected:

Fuse Amperes	Voltage
2 A	115 Vac
1 A	230 Vac

With an input of 115 Vac (230 Vac if so equipped) ±5 percent, 50 to 60 Hz, check the following at the Power Supply PCB edge-connector, P103.

Table. 4-2: Power Supply Voltage Checks.

	Volts	Pin	Ground
1.	210 V ±25 percent at	pins V, 18	(GND 20, X)
2.	21 V ±20 percent at	pins S, 15	(GND BLACK TEST POINT)
3.	9 V ±20 percent at	pins Y, 21	(GND BLACK TEST POINT)
4.	-9 V ±20 percent at	pin 2	(GND BLACK TEST POINT)
5.	-21 V ±20 percent at	pin 4	(GND BLACK TEST POINT)

Table. 4-3: Power Supply Adjustments.

	Voltage	Test Point	Ground	Adjust
1.	15 Vdc ±0.3	BLUE	BLACK	R5 (15 Vdc ADJ)
2.	-15 Vdc ±0.3	VIOLET	BLACK	R5 (15 Vdc ADJ)
3.	5 Vdc ±0.3	RED	BLACK	R19 (5 Vdc ADJ)
4.	-5 Vdc ±0.3	GREEN	BLACK	R19)5 Vdc ADJ)

4.4.3. Oscillator Adjustment

The accuracy of the oscillator may be determined, relative to a frequency standard, by observing the rate of drift of an oscilloscope pattern as shown in Figure 4-1, the oscillator accuracy test diagram.

If the pattern moves to the right, the frequency of the oscillator under test is lower than that of the frequency standard; if the pattern moves to the left, the frequency under test is too high.

To check oscillator frequency (not stability):

1. Trigger the oscilloscope externally with the 1 MHz standard.

2. Connect a 1 MHz frequency from the Model 8120 to the vertical input of the oscilloscope, (pin X of the Time Base PCB).

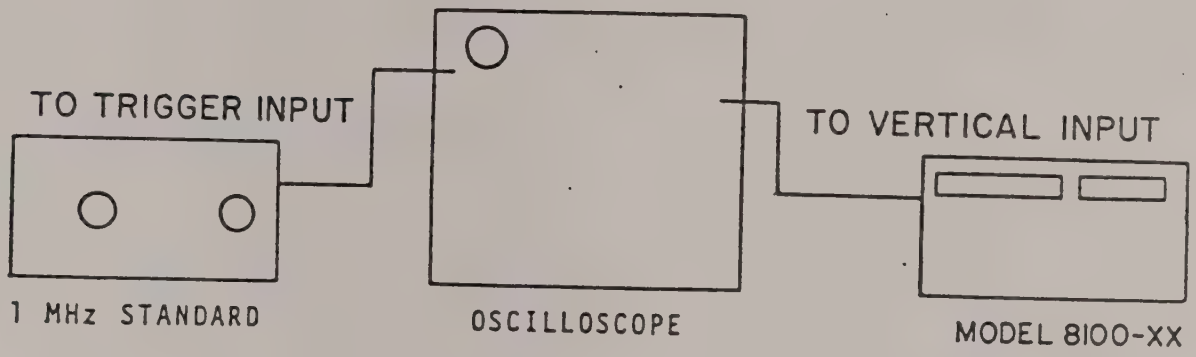
3. Set the oscilloscope sweep time to 0.1 us/cm and adjust the controls to obtain a presentation of one to two cm vertical deflection.

4. Horizontal drift of the oscilloscope display in cm/sec is the difference from the standard frequency in parts/10 -7. If necessary, adjust the oscillator (C3, on the Time Base PCB) until drift is negligible.

Table. 4-4: Oscillator Accuracy.

Drift	Accuracy
1 cm/0.1 s	1 part in 10 to the -6
1 cm/s	1 part in 10 to the -7
1 cm/10 s	1 part in 10 to the -8
1 cm/100 s	1 part in 10 to the -9

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
—	RELEASED	4-16-85	OR
A	REVISED PER ECO 7613	7-24-85	OR



	8154
	8155
NEXT ASSY	USED ON
APPLICATION	

TOLERANCES
UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:
Figure 4-1

ENGR	[signature]	4/15/85
CHECK	[signature]	4-16-85
DRAWN	[signature]	4/16/85

AUSTRON INC.
AUSTIN, TEXAS

BLOCK DIAGRAM- OSCILLATOR ACCURACY TEST

SIZE	CODE IDENT NO.		REV
1	24672	12410260	A

SCALE NONE

SHEET 1 OF 1

4.4.4. Generate Function

1. Place the mode selection switch in GENerate position and ensure that the DISPLAY indexes are in a normal sequence.

2. Preset 23 hours 59 minutes 59 seconds into the TOD Accumulator and note that on the next count the display will become all ZEROs (and, if the instrument displays days, that the days register advances one count).

3. If the Days/ID option is installed, repeat Step 2 with 009 in the DAYS/ID Accumulator and observe that on the next count the DAYS/ID Accumulator will advance to 010.

4. Repeat Step 3 to ensure the correct operation of the remaining digit of the days accumulator.

4.4.5. Shaper & Modulator
(Dwg. No. 12302556-5)

1. Adjust TUNE control for maximum ac signal at the MOD test point.

2. Adjust MOD R20 control for a nominal 3 Vp-p output of the Large Cycle signal.

3. Adjust RATIO R16 control for a 3:1 modulation ratio.

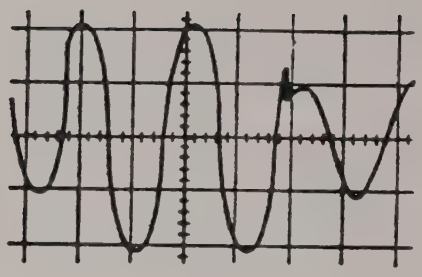
4. Return to the TUNE control and adjust until the junction point of the large and small cycles has a minimum of distortion (refer to Figure 4-2).

5. Adjust DC CODE R23 amplitude control for a nominal output of 6 Vp-p.

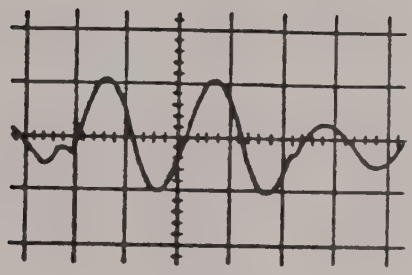
4.4.6. General Checkout

No additional adjustments are required in the instrument. To facilitate tracing possible malfunctions, determine if each plug-in PCB is performing in accordance with the circuit description provided in other sections of this manual. It is advisable to determine proper operation of the PCBs in the order of decreasing signal repetition rate.

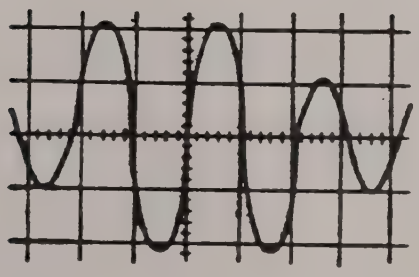
REVISIONS			
LTR	DESCRIPTION	DATE	APPD
	RELEASED	11/15/85	CRL



Incorrect
Adjust Tune Control CW



Incorrect
Adjust Tune Control CCW



Correct

		TOLERANCES UNLESS OTHERWISE SPECIFIED			AUSTRON INC. AUSTIN, TEXAS	
		DEC	FRAC	ANG		
		MATERIAL: Figure 4-2			TUNE CONTROL ADJUSTMENT	
	8100	Q.A.			SIZE 1	CODE IDENT NO. 24672	12408760	REV —
NEXT ASSY	USED ON	ENGR						
		CHECK	[illegible]	11-16-85				
APPLICATION		DRAWN	P.J. [illegible]	11-15-85	SCALE NONE		SHEET 1 OF 1	

5. FUNCTIONAL DESCRIPTION

5.1. SCOPE OF SECTION

Section Five includes detailed explanations of the Model 8120 circuit functions, with assembly drawings, logic and schematic diagrams, and parts lists for each circuit of the basic unit. Also included is a basic unit block diagram.

Schematics and specific PCB assembly descriptions relating to the basic unit are provided at the end of the chapter. Standard options, when included, are described in Chapter Six. Special modifications, if any, are presented in Chapter Seven.

The basic Model 8120 Time Code Generator is a digital clock which generates a serial time code. An internal 1 MHz time base signal is divided down to 1 pps and fed to a TOD (Time-of-Day) which outputs parallel, BCD time in hours, minutes and seconds. The accumulated time is displayed and fed through buffers to a rear panel connector. This same time information is serialized, buffered and fed to rear panel BNC connectors in both DC Level Shift form and in a modified IRIG B format modulating a 1 kHz carrier. Four simultaneous pulse rates are also available at the rear panel connector.

Provision is included for mode of operation selection and for manual entry of the start time.

The above circuitry is described in this chapter under the following headings and in more detailed circuit descriptions at the end of the chapter.

1. Overall Functional Descriptions
   a. Time Base and Control
   b. Minor Counter
   c. TOD Accumulator
   d. Buffer
   e. Code Generator
   f. Modulator

2. Display

3. Power Supply

The reference designators used in the Model 8120 are listed in Table 5-1.

Table. 5-1: Reference Designators.

Symbol	Component
A	Printed Circuit Board (PCB)
C	Capacitor
CR	Diode
DS	Lamp
FL or Z	Filter
F	Fuse
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
U	Integrated Circuit (IC)
UQ	Transistor Pack
UR	Resistor Pack
S	Switch
T	Transformer
TP	Test Point
W	Jumper
X	Socket

5.2. OVERALL FUNCTIONAL DESCRIPTIONS

Refer to the basic generator block diagram (Dwg. No. 12305008-04).

5.2.1. Time Base/Serial Preset-Reset (A27) (Dwg. No. 12302566-15)

Referring to the block diagram, the Time Base and Control PCB is shown at the lower left. This PCB contains the 1 MHz internal oscillator with shaper, the Start/Stop flip-flop, the Elapsed Time gate and a three-decade divider. The symmetrical 1000 kpps (5 x 10 to the -4) output from the Divider is fed to the Modulator PCB where it is shaped to form the 1 kHz carrier for the modulated time code. The inverse of this signal (5 x 10 to the -4) is fed through an inverting buffer on the Modulator PCB to a rear panel connector as the 1000 pps pulse rate. The (8 x 10 to the -4) output is fed to the Minor Counter and Code Generator.

5.2.2. Minor Counter (A25) (Dwg. No. 12302632-02)

The Minor Counter is a three-decade divider equipped with parallel preset inputs and two sets of buffered parallel, BCD outputs. The 1 kpps (8 x 10 to the -4) input from the Time Base is fed through an Update Inhibit circuit to the divider where it is divided down to 1 pps (8 x 10 to the -1). This signal is fed to the TOD Accumulator and Code Generator PCBs. In addition, three pulse rates (100 pps, 10 pps, and 1 pps) with ten percent duty cycle are developed on the Minor Counter PCB.

5.2.3. TOD Accumulator (A23) (Dwg. No. 12302543-03)

The Tod Accumulator accepts the 1 pps (8 x 10 to the -1) output from the Minor Counter and divides it into units and tens-of-seconds, units and tens-of-minutes and units and tens-of-hours. The decade and scale-of-six dividers which accomplish this can be parallel preset, as well as provide parallel BCD outputs. This permits the time set on the front panel PRESET switches to be entered under the control of the PRESET/RESET switch. The parallel BCD outputs are fed to:

1. The Display Assembly
2. The Code Generator
3. Through Buffers to provide TOD Outputs through a rear panel connector.

5.2.4. Code Generator (A22)
(Dwg. No. 12302554-01)

The Code Generator accepts the parallel BCD inputs and develops a serial level shift code complete with index and frame markers. Days/ID are replaced by zeros in the code, in the absence of this option. The level shift code is fed to the Modulator.

5.2.5. Modulator (A20)
(Dwg. No. 12302556-05)

The Modulator contains circuitry which modulates a synchronized 1 kHz sine wave with the serial level shift code from the Code Generator. The 1 kHz sine wave is developed by shaping the (5 x 10 to the -4) input from the Time Base previously mentioned. The modulated and level shift (DC) codes are buffered; then, fed to rear panel connectors. Adjustments for mark-to-space Ratio and Amplitude are provided.

5.2.6. Power Supply (A101)
(Dwg. No.12304810-09)

The power supply is described in detail in the following section.

5.2.7. Display Assembly (A102)
(Dwg. No. 12304945-02)

The six-digit in-line, in-plane display indicates TOD in hours, minutes and seconds. It includes provision for expansion to nine digits by the addition of Days/ID.

5.3. CIRCUIT DESCRIPTIONS

The circuit descriptions contained in this chapter are used in several AUSTRON Models. As a result, references may be made to control lines, circuits or functions which are not applicable to the Model 8120. Notable references to PRESET and GENERATE circuits (although contained, in part, on some of the PCBs), are inoperative and these sections should be disregarded.

Table. 5-2: Circuit Description Index Information.

Location	Description	Schematic #	Page #
A1 - A19	Reserved for Options		
A20	Modulator	12302556-05	5-33
A21	Days Accumulator (option)	12302632-21	6-5
A22	IRIG DC Code Generator	12302554-01	5-27
A23	TOD Accumulator	12302543-03	5-17
A24	Buffer	12302535-03	5-22
A25	Minor Counter	12302632-02	5-13
A26	Reserved for options		
A27	Time Base/Serial Preset-Reset	12302566-15	5-39
A101	Power Supply	12304810-09	5-46
A102	Display Assembly	12304945-02	5-54

All plug-in modules are designed so that the PCB will only fit into position if it is correctly aligned; however, caution must be exercised to ensure that a PCB is installed in the correct slot. Extractor handles on all PCBs are numbered to facilitate correct installation.

CAUTION

When mounting a PCB on the extender PCB, it is possible to install the PCB backwards which will result in serious damage.

REVISIONS					
ITEM	DESCRIPTION	INC NO	ECO NO	DATE	APP'D
A	RELEASE TO RECORDS				
B	DWG NO. WAS 05100501		0837		
C	FAN WAS WIRED TO J102-16-2		7101	2/7/83	CL
D	REVISED PER ECO 8158 PH			11-23-83	VL

A101
POWER SUPPLY
SCH: 12304310-9
ASSY: 10304810-9

J102

A21-25 ← GRD
A20-25 ← GRD
A23-25 ← SENSE RET
A20-24 ← +5V
A27-24 ← +5
A23-24 ← 15 SENSE
+15V
-15V

B1 FAN

P/O S3
SHOWN IN POS. 1,
"POWER OFF"

+5V
+210V RET
+210V UNREG.

A102
DISPLAY ASSEMBLY
1230494S-2 SCH
1030494S-2 ASS'Y

SECONDS | MINUTES | HOURS | DAYS/ID

1S 2S 4S 8S 10S 20S 40S 1M 2M 4M 8M 10M 20M 40M 1H 2H 4H 8H 10H 20H 1D 2D 4D 8D 100 200 400 800 1000 2000 4000 8000

A22-XA22
CODE GENERATOR
SCH: 12302559-1
ASS'Y: 10302559-1

SEE NOTE 2

A24-XA24
BUFFER
SCH: 12302535-3
ASS'Y: 10302535-3

1SB 2SB 4SB 8SB 10SB 20SB 40SB 1MB 2MB 4MB 8MB 10MB 20MB 40MB 1HB 2HB 4HB 8HB 10HB 20HB

J3
55I306-0031

BCD OUT/SEARCH CONTROL

A25-S ← 10 PPS
A25-H ← UPDATE INHIBIT

J9 CODE OUT
J10 DC CODE
J13 I.D. UPDATE
P/O E13 OPT
J4
57-40140

A20-XA20
MODULATOR
SCH: 12302554-3
ASS'Y: 10302554-5

SERIAL CODE
-15V
+15V

1 PPS
100 PPS
10 PPS
UPDATE INHIBIT
ELAPSED TIME
+15
PULSE RATE

A27-XA27
TIME BASE
SCH: 12302544-3 ASSY 12302544-15

INT
EXT
S1
J12
EXT 1MHz

A25-XA25
MINOR COUNTER
SCH: 12302632-2
ASS'Y: 10302632-2

SEE NOTE 1
+5V
R1 1K
R2 1K
RESET TIME
PRESET TIME

A23-XA23
TOD ACCUMULATOR
SCH: 12302543-3
ASS'Y: 10302543-3

1248 S6 Y | 124 S7 Y | 1248 S8 Y | 24 S9 Y | 1248 S10 Y | 12 S11 Y
SEC | MIN | HRS

S4A

A21-XA21
DAYS ACCUMULATOR
SCH: 12302632-21
ASS'Y: 10302632-21

1248 S12 Y | 1248 S13 Y | 1248 S14 Y
DAYS/ID

RESET DAYS
PRESET DAYS
S4B

1DB 2DB 4DB 8DB 10DB 20DB 40DB 80DB 100DB 200DB 400DB 800DB

P/O E13 OPT

S3: (ROTARY)
1 POWER OFF
2 STOP
3 HOLD
4 GEN

S4: (MOMENTARY)
1. RESET
2. PRESET

S3 A B

S15
P/O E13 OPT
365 366 ID

1MSB 2MSB 4MSB 10MSB 20MSB 40MSB 100MSB 200MSB 400MSB 800MSB

J6
55I306-0005
BCD MS
E14 OPTION

NOTES:
1.) TO SEPARATE SIGNAL GRD FROM CHASSIS GRD, CUT GRD LUG AT A23.
2.) REMOVE GRD WHEN E13 OPT 15 INSTALLED
3.) +5V CONNECTION ON CAF PINS 24&33.
GND CONNECTION ON CAF PINS 22&CC.

5-6

LIST OF MATERIALS

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

DRAWN 7-1-82 DATE
CHECK DATE
ELECT. DATE
MECH DATE
PROJ. ENG. 7/6/82 DATE
Q.A. DATE
MFG. + ENG. NEXT ASSY
SCALE 1 DO NOT SCALE
DWG SIZE D

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
.X ±
.XX ±
XXX ±
ANGLES ±
MATERIAL
REV

AUSTRON INC
AUSTIN, TEXAS
CODE IDENT. 24577

BLOCK DIAGRAM
MODEL 8120
1216B WITH
E13 & E14
OPTIONS.

DWG NO. 12305003-6 ISH 1

ASSEMBLY SHIPPING ASSY 8120
ASSEMBLY NUMBER 30605008-4
REFERENCE DESIGNATOR PREFIX
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
1	FINAL ASSY 8120	25605013-2		24672
1P3	CONN 50 PIN PLUG	551306-0050	57-30500	02660
1P4	CONN 14 PIN PLUG	551306-0000	57-30140	02660
1W1	POWER CORD, (SPECIAL)	570076-0002	17250	70903
MP1	SUPPORT REAR	00400951-2		24672
MP2	SUPPORT REAR	00400951-2		24672

ASSEMBLY FINAL ASSY 8120
ASSEMBLY NUMBER 25605013-2
REFERENCE DESIGNATOR PREFIX 1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PANEL ASSY, FRONT 8120	10904991-1		24672
A2	PANEL ASSY, REAR 8120	10904815-7		24672
A3	CHASSIS CKT. ASSY 8120	20606350-2		24672

ASSEMBLY PANEL ASSY, FRONT 8120
ASSEMBLY NUMBER 10904991-1
REFERENCE DESIGNATOR PREFIX 1A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
MP1	WINDOW	02005001-1		24672
S2	ROTARY SWITCH ASSY	12006344-14		24672
S2MP1	KNOB BAR RNG SKRT 1/4H .70D	505001-0020	70B-2-2G	07933
S4	SW, TOGGLE DPDT ON-OFF-ON MIN	553304-0013	7205SYZQ	09353
S6	SW, THUMBWHEEL BCD COMP ONLY	553101-0008	29102/B	07126
S7	SW, THUMBWHEEL BCD COMP ONLY W/COL	553101-0007	29102/B W/COLON	07126
S8	SW, THUMBWHEEL BCD COMP ONLY	553101-0008	29102/B	07126
S9	SW, THUMBWHEEL BCD COMP ONLY W/COL	553101-0007	29102/B W/COLON	07126
S10	SW, THUMBWHEEL BCD COMP ONLY	553101-0008	29102/B	07126
S11	SW, THUMBWHEEL BCD COMP ONLY W/COL	553101-0007	29102/B W/COLON	07126
S12	SW, THUMBWHEEL OPTIONAL			
S13	SW, THUMBWHEEL OPTIONAL			
S14	SW, THUMBWHEEL OPTIONAL			

ASSEMBLY PANEL ASSY, REAR 8120
ASSEMBLY NUMBER 10904815-7
REFERENCE DESIGNATOR PREFIX 1A2
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
B1	FAN AXIAL DC 24 V 3 W 36 CFM	570899-0011	8124K	23936
B1MP1	GUARD FINGER 3.12 SQ. FAN	570899-0005	5508	23936
J3	CONN 50 PIN SOCKET	551306-0051	57-40500	02660
J4	CONN 14 PIN SOCKET CHASSIS RCPT	551306-0005	57-40140	02660
J9	CONN, BNC	551100-1094	UG-1094A/U	74868
J9MP1	WASH FIBER FLAT .380.X630X.016	510900-0016	F-7716-380	61000
J9MP2	INSULATOR UG 1094/U BNC	520025-1094	10221N	07047
J10	CONN, BNC	551100-1094	UG-1094A/U	74868
J10MP1	WASH FIBER FLAT .380.X630X.016	510900-0016	F-7716-380	61000
J10MP2	INSULATOR UG 1094/U BNC	520025-1094	10221N	07047
J12	CONN, BNC	551105-1094	UG-1094A/U	74868
J12MP1	WASH FIBER FLAT .380.X630X.016	510900-0016	F-7716-380	61000
J12MP2	INSULATOR UG 1094/U BNC	520025-1094	10221N	07047
S1	SW, SLIDE SPDT 125V	553007-0005	GF-124-SPDT	79727

MANUAL PARTS LIST MODEL 8120

09 DEC 85

ASSEMBLY CHASSIS CKT. ASSY 8120
ASSEMBLY NUMBER 20606350-2
REFERENCE DESIGNATOR PREFIX 1A3
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A20	PCB SHAPER & MODULATOR	10302556-5		24672
A22	PCB ASSY CODE GENERATOR	10302554-1		24672
A23	PCB ASSY TOD ACCUMULATOR	10302543-3		24672
A24	PCB ASSY, 20 BIT BUFFER	10302535-3		24672
A25	PCB ASSY 3 DIGIT ACCUMULATOR W/BUF	10302632-2		24672
A27	PCB ASSY T.B. SERIAL PRESET/RESET	10302566-15		24672
A29	PCB ASSY EXTENDER	10302507-1		24672
A101	ASSY POWER SUPPLY	23604810-9		24672
A102	ASSY DISPLAY 6 DIGIT	12004945-2		24672
P102	HOUSING, PLUG 5 PIN	551117-0005	03-06-2055	27264
J1	PIN MINI MALE	551117-0060	02-06-2103	27264
J2	PIN MINI MALE	551117-0060	02-06-2103	27264
J3	PIN MINI MALE	551117-0060	02-06-2103	27264
J4	PIN MINI MALE	551117-0060	02-06-2103	27264
J5	PIN MINI MALE	551117-0060	02-06-2103	27264
R1	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R2	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
XA20	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA22	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA23	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA24	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA25	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA27	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA29	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA101	CONN 22 POS DUAL LUG	551009-0022	50-44A-30	71785

5.3.1. Minor Counter (Three Digit Accumulator) (Schematic Dwg. No. 12302632-02)

The Minor Counter PCB can provide two serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three, four-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update-inhibit circuit. Provision is included for three output pulse rates with ten percent duty cycle which may be supplied in place of the days cycle circuit.

5.3.1.1. Decade Divider Circuits

The three decade dividers are connected in tandem. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe (PRESET) line is grounded. Jumper W2 permits the data strobe associated with the first decade (U4) to be wired in common with the data strobe input to the second decade (U6). The decade zero-reset inputs are wired in common through buffers on (U8) to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

5.3.1.2. Output Buffer Circuits

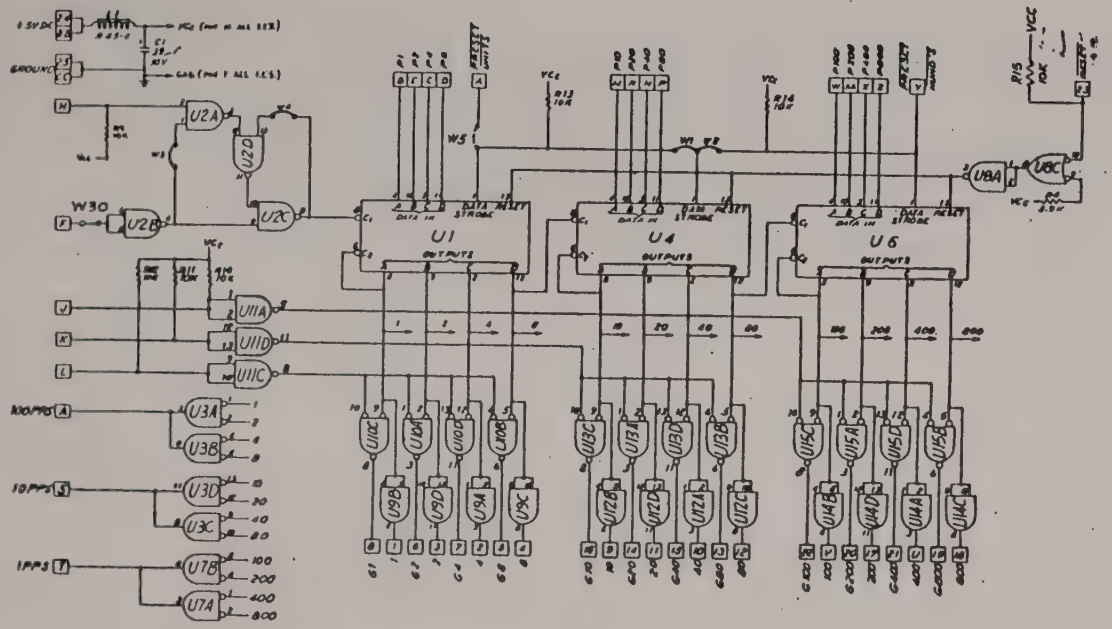
The BCD output buffers are non-inverting. One of the two sets (U10, U13 and U15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters on (U11).

5.3.1.3. Output Pulse Rate Circuits

Three sets of gates are used to produce three, ten percent duty cycle pulse rates. Each pulse goes high when the four outputs from the corresponding decades are low (leading edge on-time). The pulse remains up until the output of the decade is 001. Thus, the pulse is high ten percent of the time. The output is a 5 Vdc logic level behind 6 kilohm.

The pulse rate outputs are fed to pins A, S and T.

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO	DATE	APPD
	B	ADDED R13, 14 & 15	632	12/72	JM
	C	U1, 4 & 6 WERE N8280P	17102	7/9/80	JM
	D	DELETED R1, R2 & C2; ADDED W30	17751	7/21/82	JM
	E	DWG NO. WAS 21632-7-2	4837		
	F	CHG'D. I.C. REF DES FROM 'A' TO 'U'	6557	9-19-84	OK



1. I.C. TYPES AS FOLLOWS:
U1, 4 & 6 = SN74LS374N
U2 & 11 = MC846P
U3 & 7 = MC1810P
U8 = SN7400N
U9, 12 & 14 = MC1806P
U10, 13 & 15 = MC1808P

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO.
	8154 A19		

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DEC | FRAC | ANG

MATERIAL:

ENGR	G.M.	5-30-73
CHECK	S-D	5-73
DRAWN	Z	5-73

AUSTRON INC
AUSTIN, TEXAS

SCHEMATIC, 3-DIGIT ACCUMULATOR BUFFER

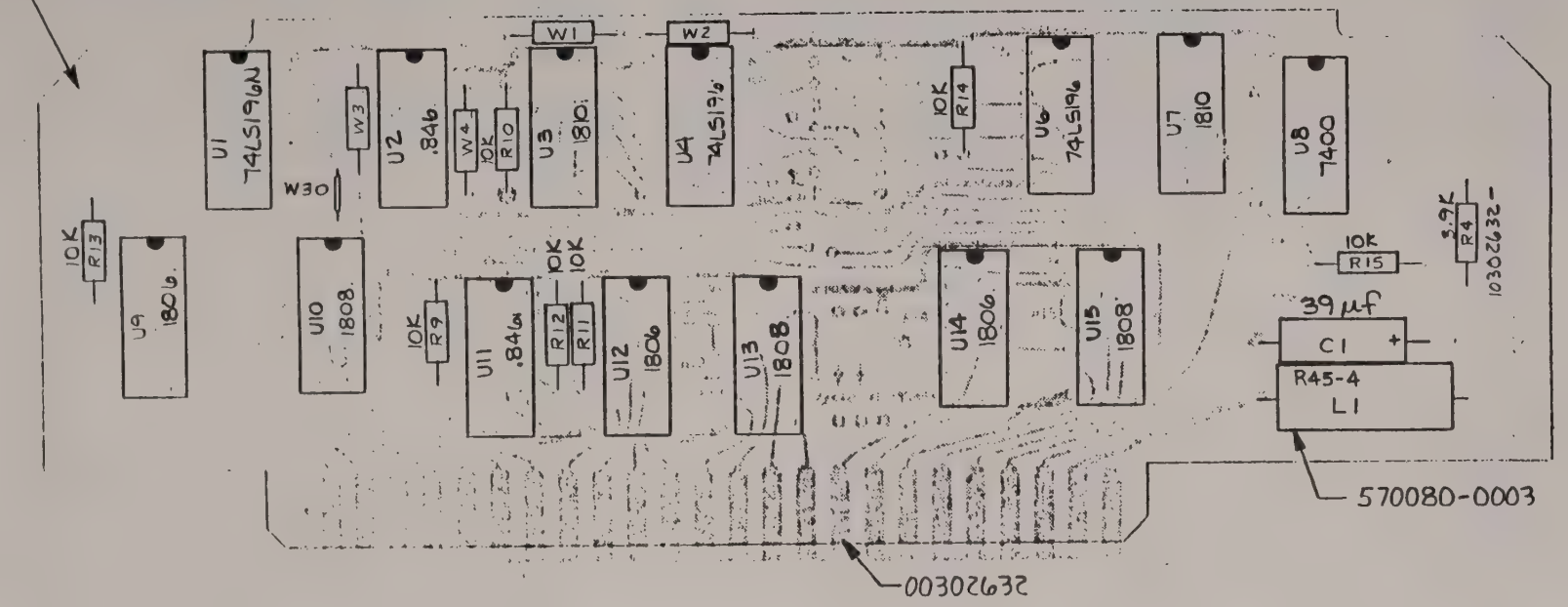
SIZE	CODE IDENT NO.		REV
2	24672	12302632-2	F

SCALE | SHEET OF

5-13

F	RELEASED TO RECORDS			
G	DWG WAS0216 32-4-2 ECO 4837			
H	REVISED PER ECO			
J	REVISED PER ECO 7077			
K	REVISED PER ECO 7185			

INSTALL 50620-2030, NOT SHOWN
(2 PLACES)



B159	A19	JK 7-21-82	AUSTRON INC. AUSTIN, TEXAS
		24672	PCB ASSY, 3 DIGIT ACCUMULATOR W/BUFFER
		2:1	5-14
			10302632-2 K

ASSEMBLY PCB ASSY 3 DIGIT ACCUMULATOR W/BUF
ASSEMBLY NUMBER 10302632-2
REFERENCE DESIGNATOR PREFIX 1A3A25
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	220 PF 500V 5 CAP DIP MICA	603000-0221	CM05FD221J03	09023
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 82 K 1/4W 10%	651102-0823	RC07GF823K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R4	RES FXD COMP 3.9 K 1/4W 10%	651102-0392	RC07GF392K	81349
R9	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R10	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R11	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R12	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R13	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R15	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
U2	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U3	IC QUAD 2-IN NOR GATES	703MC1810P	MC1810P	04713
U4	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
U6	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
U7	IC QUAD 2-IN NOR GATES	703MC1810P	MC1810P	04713
U8	IC QUADR 2-INP NAND GATE	703SN7400N	SN7400N	01295
U9	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U10	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713
U11	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U12	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U13	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713
U14	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U15	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713
W1	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W2	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W3	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W4	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210

5.3.2. Time Of Day Accumulator (Schematic Dwg. No. 12302543-03)

The Time of Day Accumulator PCB successively divides an incoming 1 pps signal providing outputs which represent seconds through hours. The PCB buffers all output signals and includes an input inhibit circuit. One second after reaching 23:59:59, the dividers recycle to zero.

5.3.2.1. Divider Circuits

Dividers (U1), (U4), (U7) and (U8) are divide-by-ten circuits. Dividers (U3) and (U5) are divide-by-eight circuits. Recycle circuits formed from gates on (U13) and (U17) convert U1 and (U3) to a scale of sixty, (U7) and (U8) to a scale of sixty, and (U7) and (U8) to a scale of twenty-four. Each divider has its data input, connected to a preset time source. Grounding the appropriate preset line loads the preset time into divider. Grounding pin 23 resets the accumulator through gates on (U9), (U13) and (U17).

5.3.2.2. Recycle Circuits

The scale-of-sixty recycle circuits for seconds and minutes are identical. The seconds circuit consists of AND gate (U13,3) and a differentiating circuit formed from C3, R4 and R5. Gate (U13,9) output goes high when (U3) reaches a count of five. The gate resets (U1) and (U3) through C3 and (U13,6) when it returns low at the next count.

The scale-of-twenty-four recycle circuit for hours consists of AND gates (U13,8), (U17,8) and a differentiating circuit formed from C5, R9 and R10. The output from (U17,8) goes high when (U7) and (U8) reach a count of twenty-three. Gate (U17,8) resets (U7) and (U8) through C5 and (U9,8 and 6) in tandem when it returns low at the next count.

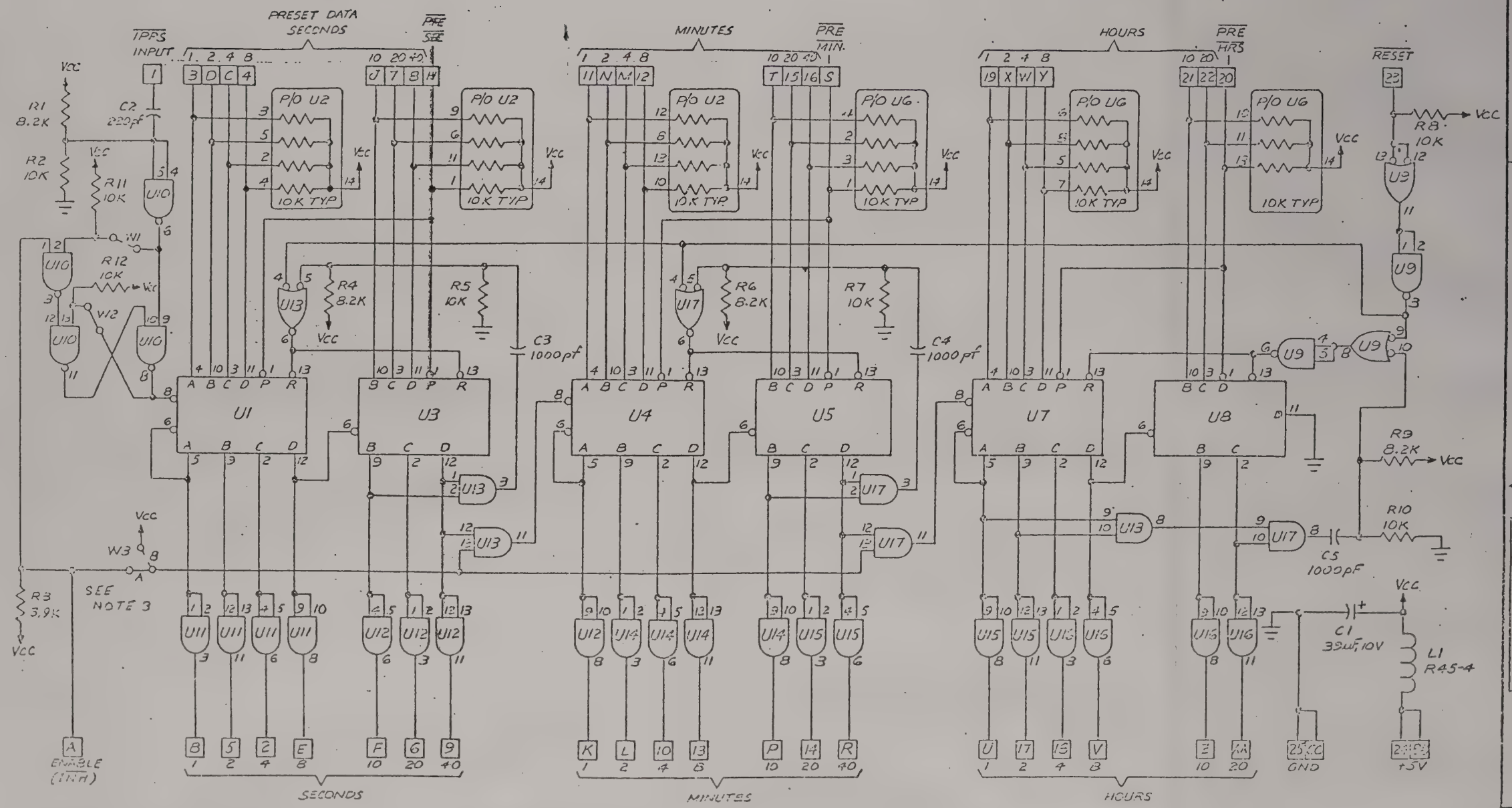
5.3.2.3. Inhibit Circuit

The inhibit circuit stops updating of the accumulator when the unit is in HOLD. Gate (U10,6) inverts the 1 pps input.

Gates (U10,8,11) form an RS flip-flop. Gate (U10,3) inverts the INHIBIT/ENABLE line from pin A. Grounding pin A latches the flip-flop to high. The output will go low the first time the input is low after the ground has been removed from the INHIBIT/ENABLE input.

Placing jumper W3 in the B position, in clocks and generators, allows the ENABLE input at pin A to be used for HOLD.

REVISIONS					
REV	DESCRIPTION	BY/ID	NOTICE	DATE	APPROVED
D	REFER TO E.C.O		7220		
E	C3, C4, C5 (1206 pkt.) WERE 220pf.	-	17340	5/17/31	
F	NOTE 2: U10 (54S) WAS 74LS00N -	-	17453	5/23/81	
G	DWG NO. WAS 021E43-7-3		4238		



NOTES:

1. RESISTORS ARE 1/4W, 5%, CARB. COMP.
2. I.C.'S

		Vcc	GND
U1, U4, U7, U8	74LS193	16	7
U2, U6	RES. PACK (10K)	14	-
U3, U5	74LS197	14	7
U9	74LS132	14	7
U10	946	14	7
U11, U12, U13, U14, U15, U16, U17	7408	14	7

3. PROGRAMMING JUMPER W3 IS INSTALLED IN THE "A" POSITION IN READERS & READER/GENERATORS TO PREVENT UPDATE OF HOURS / MINUTES IN REVERSE READ. IT IS INSTALLED IN THE "B" POSITION IN CLOCKS & GENERATORS WHERE THE ENABLE INPUT TO PIN A IS USED FOR HOLD.

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

DRAWN	DATE 11-19-	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	AUSTRON INC. AUSTIN, TEXAS
CHECK	DATE		CODE IDENT. 24672
ELECT.	DATE		
MECH.	DATE		
PROJECT	DATE 12/		
QA	DATE		

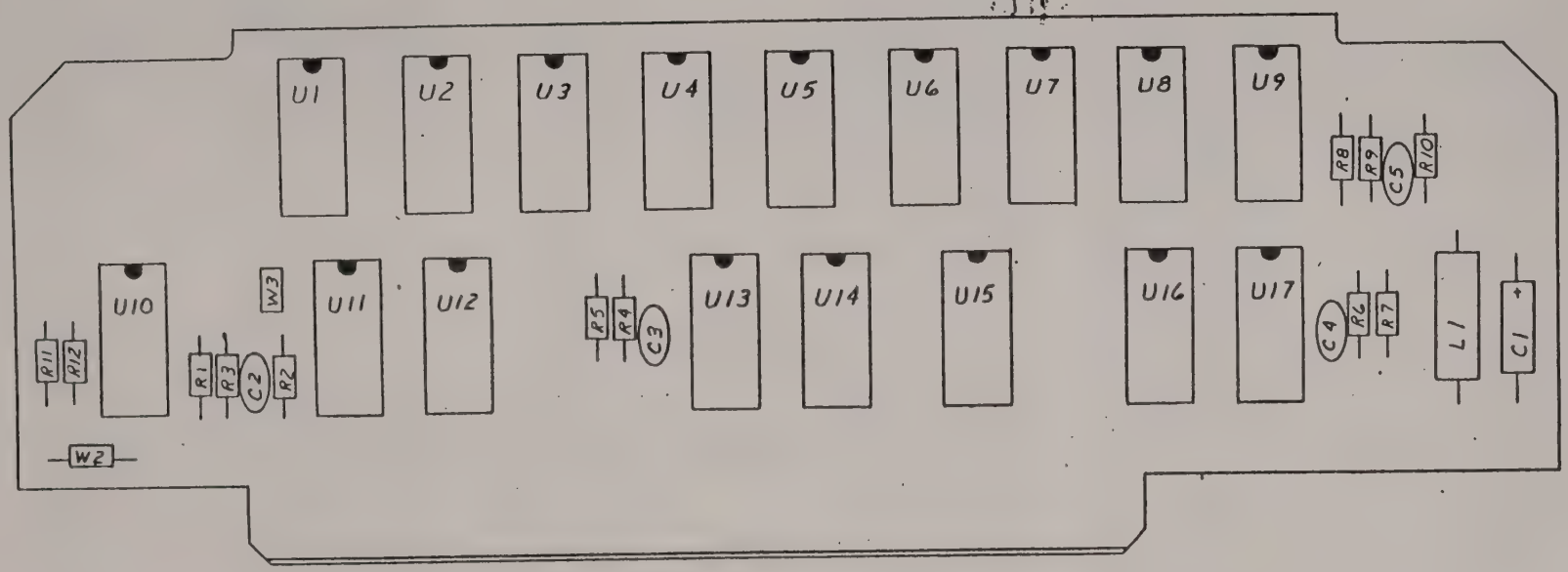
TOD ACCUMULATOR

USED ON	NEXT ASSY
APPLICATION	

SCALE	DO NOT SCALE DRAWING	SH 1 OF 1
~		

MATERIAL	DRAWING NO.			
	REF	SIZE	PART NO.	REV
5-17		C	12302543-3	G

C	REFER TO ECO		11206	10/80	Z
D	SHT. 2; C3, C4, C5 (.1 µf) WERE 220 pf.	-	17140	10/81	H. M.
E	SHT. 2: U10 (846) WAS 74LS00.	-	17439	9/81	H. M.
F	DWG NO. WAS 021543-4-3		4833		
G	P/L REVISION PER ECO 6708	-	-	9/84	OR



LIST OF MATERIALS

DRAWN	10-23-80	AUSTRON INC AUSTIN, TEXAS	TOD ACCUM. ASSY
CHECK		CODE IDENT 24672	
ENGR			
PROJ ENGR	11-80		
MFG			
QA			
USED ON / NEXT ASSY	APPLICATION	SCALE 2/1	DO NOT SCALE DRAWING
MATERIAL		DRAWING NO. B 10302543-3	REV G

5-18

ASSEMBLY PCB ASSY TOD ACCUMULATOR
ASSEMBLY NUMBER 10302543-3
REFERENCE DESIGNATOR PREFIX 1A3A23
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	CAP CERA RDL COG 220 PF 100V 5%	601110-0221	CN15A221J261	71590
C3	CAP CERA RDL COG 1000 PF 100V 5%	601110-0102	CN20A102J242	71590
C4	CAP CERA RDL COG 1000 PF 100V 5%	601110-0102	CN20A102J242	71590
C5	CAP CERA RDL COG 1000 PF 100V 5%	601110-0102	CN20A102J242	71590
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 8.2 K 1/4W 10%	651102-0822	RC07GF822K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R3	RES FXD COMP 3.9 K 1/4W 10%	651102-0392	RC07GF392K	81349
R4	RES FXD COMP 8.2 K 1/4W 10%	651102-0822	RC07GF822K	81349
R5	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R6	RES FXD COMP 8.2 K 1/4W 10%	651102-0822	RC07GF822K	81349
R7	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R8	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R9	RES FXD COMP 8.2 K 1/4W 10%	651102-0822	RC07GF822K	81349
R10	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R11	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R12	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
UR2	RES FXD DIPNET 14P 10 K 1.75W 2%	654013-0103	314A103	01121
U3	IC PRESETABLE BINARY COUNTER/LATCH	703SN74LS197	SN74LS197N	01295
U4	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
U5	IC PRESETABLE BINARY COUNTER/LATCH	703SN74LS197	SN74LS197N	01295
UR6	RES FXD DIPNET 14P 10 K 1.75W 2%	654013-0103	314A103	01121
U7	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
U8	IC PRESETABLE COUNTER/LATCH	703SN74LS196	SN74LS196N	01295
U9	IC QUAD 2-INPUT POS-NAND SCHMITT TR	703SN74LS132	SN74LS132N	01295
U10	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U11	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295
U12	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295
U13	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295

ASSEMBLY PCB ASSY TOD ACCUMULATOR (CONT)
ASSEMBLY NUMBER 10302543-3
REFERENCE DESIGNATUR PREFIX 1A3A23
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U14	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295
U15	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295
U16	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295
U17	IC QUADR 2-INP AND GATE	703SN7408N	SN7408N	01295
W2	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W3J1	CONTACT PIN	551003-0460	460-2983-02-03	71279
W3J2	CONTACT PIN	551003-0460	460-2983-02-03	71279
W3J3	CONTACT PIN	551003-0460	460-2983-02-03	71279
W3P1	JUMPER JK .100 CTR FOR .032 RND PIN	551113-0001	450-4774-01-06-10	71279

5.3.3. Buffer Assembly
(Schematic Dwg. No. 12302535-03)

The Buffer Assembly PCB contains twenty IC gates, connected as non-inverting buffers. The circuit buffers the seconds-through-hours output of the Time-of-Day Accumulators.

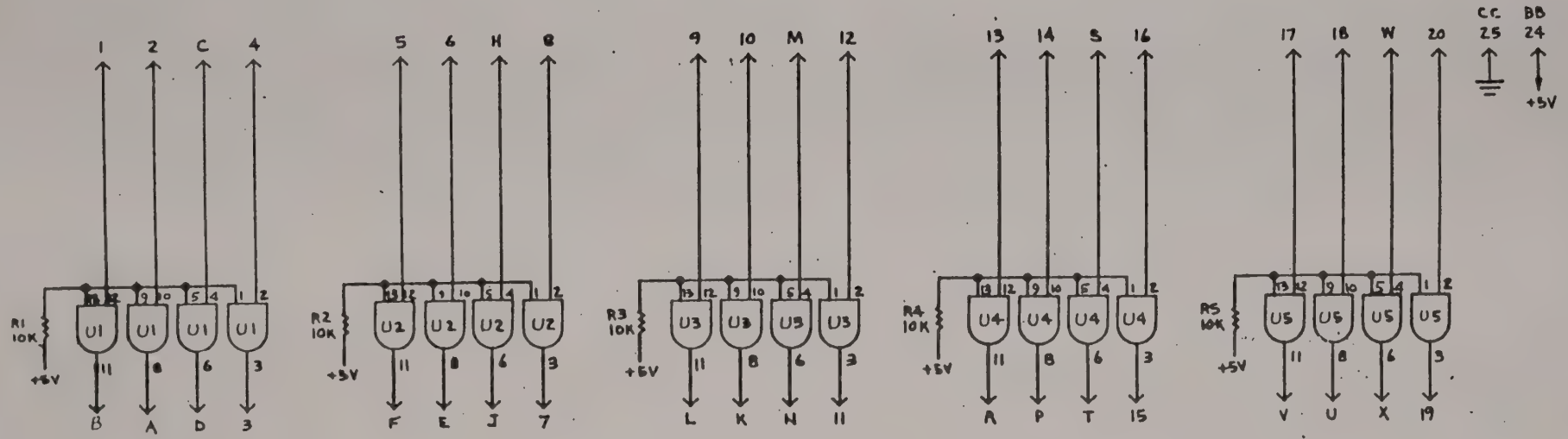
Code: 8-4-2-1

Logic: ONE = 5 Vdc $\pm$0.5 Vdc, 6 kilohm source.

ZERO = 0 Vdc $\pm$0.5 Vdc, 12 mA sink.

All outputs are short-circuit-proof to ground.

-1	UPDATED TITLE BLOCK	-	4-7	YH	
A	TRANSF. TO 2 PRINT SETS, 4 SETS EXISTING OF AL THRU AS ADDED A	-	330	4/89	
A1	SCH. NOS ARE 21535-7-16 ALSO.	-	NRC	MK	
B	DWG NO. WAS 21535-7-3		4017		

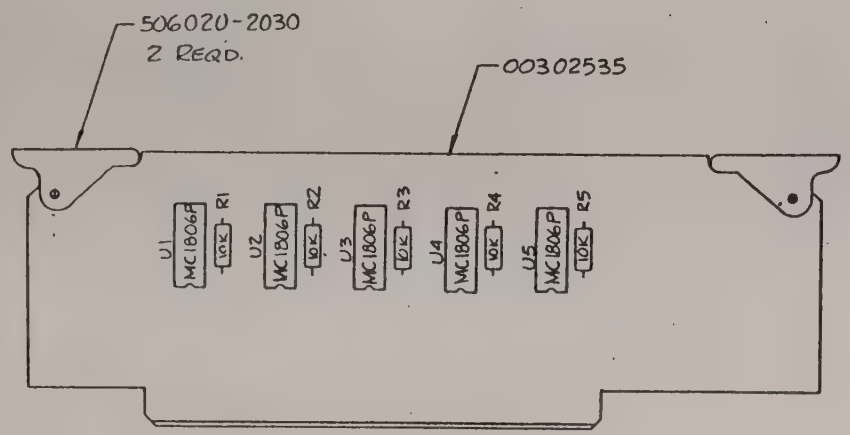


NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & " 7 " " " " " " GRD.
3. U1 THRU U5 ARE MC1B06P

B-190		AUSTRON AUSTIN, TEXAS	SCHEMATIC 20 BIT BUFFER NON-INVERTING	
SIZE			12302535-3	B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	A	DWG NO. WAS 21535-4-3 EC04837		
	B	REVISED PER ECO 6557	10/28/71	OK



5-23

NEXT ASSY	USED ON	REF DES	FIG NO.
	8190		
	8121		

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED
DEC | FRAC | ANG

MATERIAL:

ENGR	G.M.	9-68
CHECK	S-D	9-68
DRAWN	RBW	9-68

AUSTRON INC.
AUSTIN, TEXAS

PC B ASSY, 20 BIT BUFFER

SIZE	CODE IDENT NO.		REV
2	24672	10302535-3	B

SCALE 1:1 SHEET 1 OF 1

ASSEMBLY PCB ASSY, 20 BIT BUFFER
ASSEMBLY NUMBER 10302535-3
REFERENCE DESIGNATOR PREFIX 1A3A24
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R3	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R4	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R5	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U2	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U3	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U4	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U5	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713

5.3.4. IRIG DC Code Generator (Schematic Dwg. No. 12302554-01)

The IRIG DC Code Generator PCB generates the IRIG A, B, C, E, or H codes. Code selection is remotely controlled or fixed by the particular PCB configuration. Days information is optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from an external source. The following description applies in general to all configurations of the PCB. The attached assembly, schematic and parts list identifies the specific assembly.

5.3.4.1. Divider Circuits

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider (U8) is a divide-by-two, then-by-five counter which divides down the Z RATE and provides decoded outputs for the code generating gates. Divider (U15) is a divide-by-five, then-by-two counter which takes the output of (U8), divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider (U17) is a divide-by-two, then-by-six counter. (U17) controls the secondary scan gate (U4). The divide-by-twelve (U17) is used only for IRIG C, the divider being reset at the count of ten, or by the sync input for the other codes. This early reset is shown on the timing diagram as (U18,8). The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Timing Diagram (No. 12402554) is simply eliminated when the divider resets at ten. Reset-at-ten is established by gate (U18,8). A one-shot (U18,12 and 6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the PCB can supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Divider (U7), if present, is a divide-by-five counter provided for external use. It is synchronized with the other divider chips.

5.3.4.2. Scan Gate Circuits

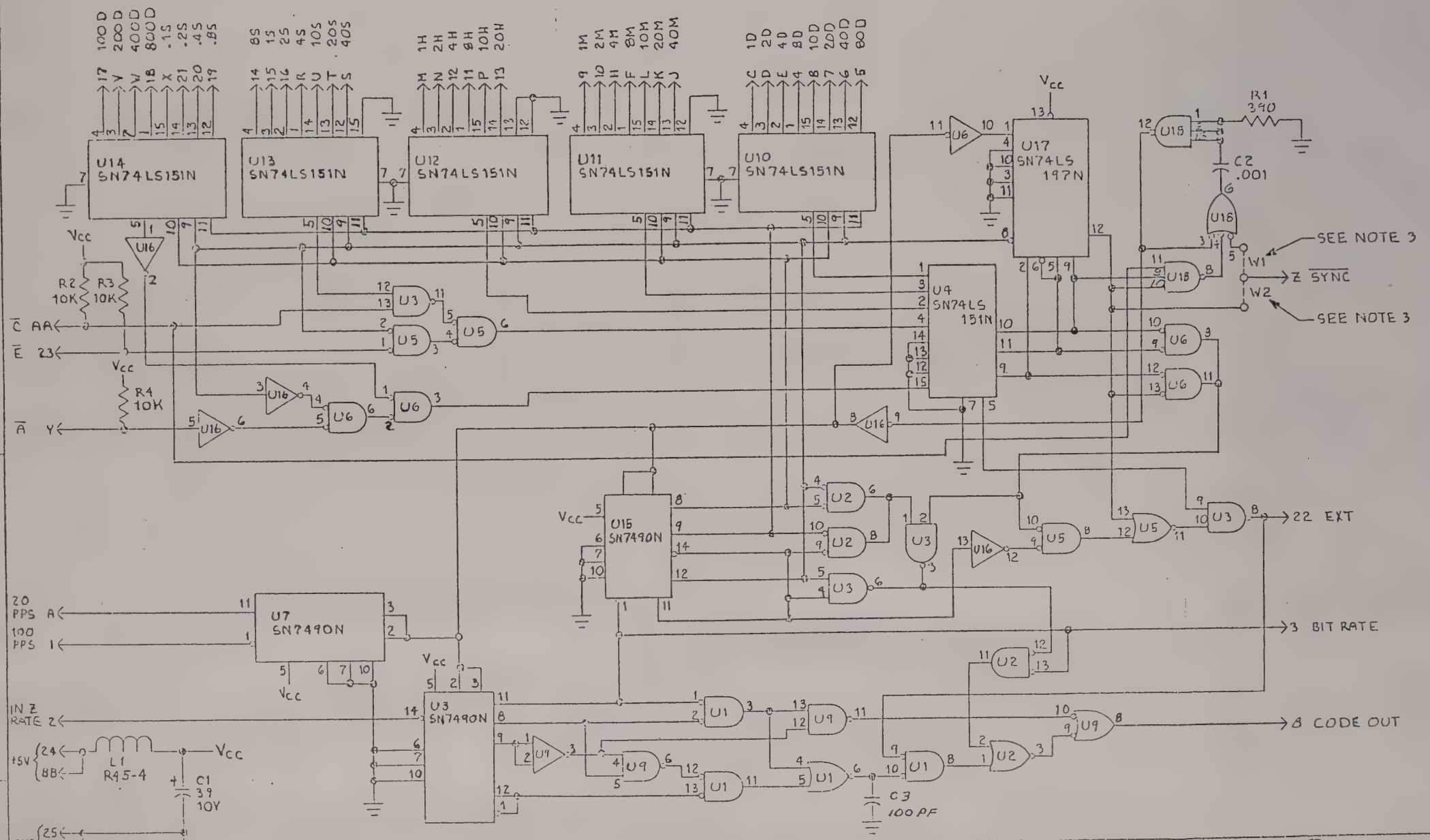
Creation of serial ONEs is accomplished by a two-stage switching network and a series of gates. Integrated circuits (U10) through (U14) are basically single-pole (pin 5 is the output), eight-position switches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular PCB configuration.) The switching is controlled by BCD information on pins 9, 10 and 11. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for switch (U4). This switch, controlled from the BCD outputs of divider (U17), selects the proper time interval for serializing each switch output. (The series of gates associated with (U14) and (U13), if present, further control these switches which may have outputs that should not be present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates (U5,8), (U5,11) and (U3,8) are used to inhibit the presence of serial ONEs at certain times when no serial ONES should be present. This prevents the spurious ONEs (coming from the switches) from appearing in this output code.

5.3.4.3. Code Generating Gate Circuits

These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the Z-RATE on pin 2. A 2 length is a ZERO, a 5 is a ONE, and an 8 is an INDEX MARKER.

The INDEX MARKERs are generated by gating the output of divider (U15). Gate (U1,3) adds information from the output of divider (U11) to create the 8 width. Gates (U6,8) and (U6,11) allow an extra pulse from gates (U2,6) and (U2,8) to give the DOUBLE-MARK at the start of the frame. Gate (U3,6) provides the MARKER at each tenth frame interval. Gate (U9,11) supplies a pulse of 2 width at the start of each bit interval. If a MARK or a ONE is not present, then the output code will be high for only the 2 width. Gate (U1,6) supplies the 5 width pulse. This is AND-gated with the SERIAL ONEs from (U3,8) by gate (U1,8). (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the 5 width to appear in the output code, masking the 2 width which is always present. Gates (U2,3) and (U9,8) are used to combine the various widths to produce the output code at pin B.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	B	REFER TO ECO396	1/81	
	C	ADDED C3 ECO [illegible]	[illegible]	
	D	ADDED R2, R3, R4 ECO 632	1/12	
	E	SN7415AN WAS DM8210 A2-4A2-5 ECO [illegible]	[illegible]	
	F	A16 WAS MC8136P WAS N8280A ECO17073		
	G	CHGD "A" TO "U" ECO17743	11/83	
	H	DWG NO. WAS 021554-1-1 ECO4837	5/84	



5. U1, U2, U5, & U6 ARE MC1810P.
   U3 & U9 ARE MC846P.
   U16 IS SN74LS04N.
   U18 IS SN7410N.
4. PIN 14 OF ALL ICs IS CONN TO Vcc.
   PIN 7 OF ALL ICs IS CONN TO GND.
3. INSTALL W1 FOR G1; W2 FOR G2.
2. CAPACITORS ARE IN MICROFARADS.
1. RESISTORS ARE IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	REF DES	FIG NO
	B155-0457	1A1A6,9,12,15,18	4-10
	8120		

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR
CHECKED
DRAWN [illegible] 1/16/81

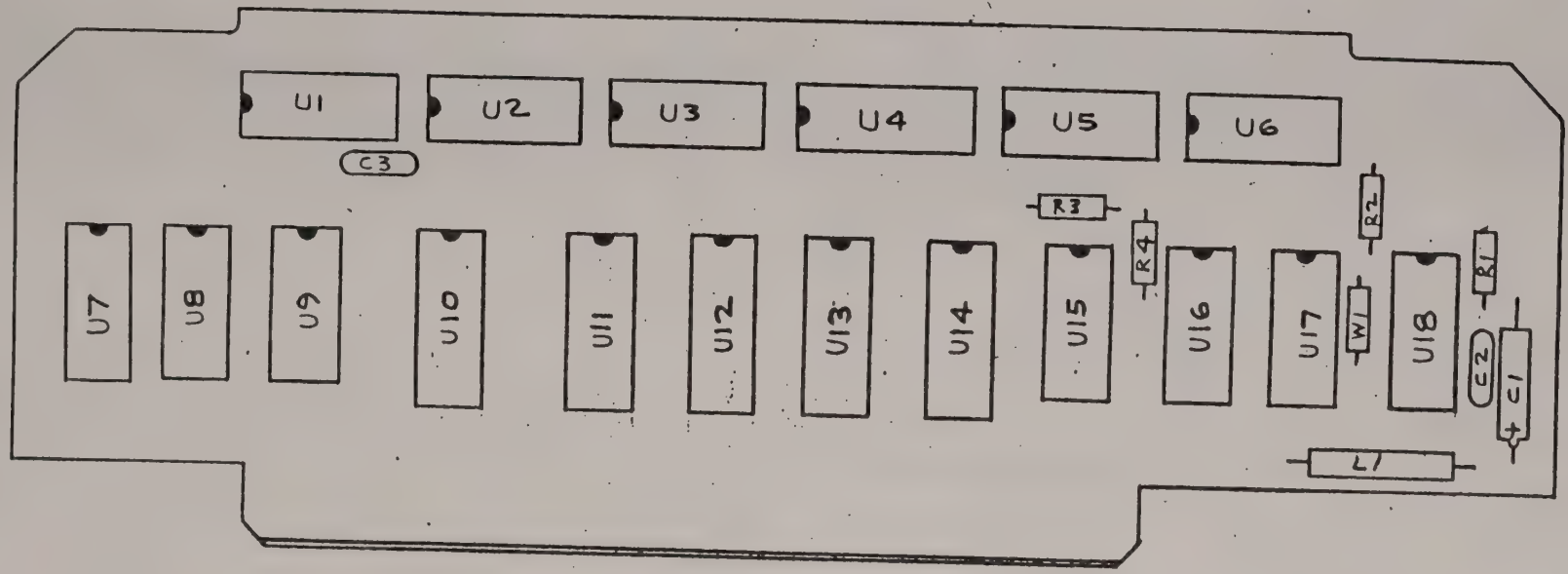
AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC,
IRIG A-B-C-E
SWITCHABLE DC CODE GENERATOR

SIZE	CODE IDENT NO		
3	24672	12302554-1	H

SCALE NONE SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	E	REDRAWN – NO CHANGES	6-1-83	
	F	CHANGED A7D U SN74LS15N WAS SN7416IAN; PER ECO 4790	11-23-83	ROB
	G	DWG NO. WAS 21554-4-1; ECO 4837	4-1-84	



25605206-10	8155-0457	1A1A6-9-12-15-18	4-10
—	—		—
NEXT ASSY	USED ON	REF DES	FIG NO.

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED: DEC | FRAC | ANG

MATERIAL:

ENGR		
CHECK		
DRAWN	Redrawn	6-1-83

AUSTRON INC
AUSTIN, TEXAS

PCB ASSY, IRIG A,B,C,D SWITCHABLE GEN

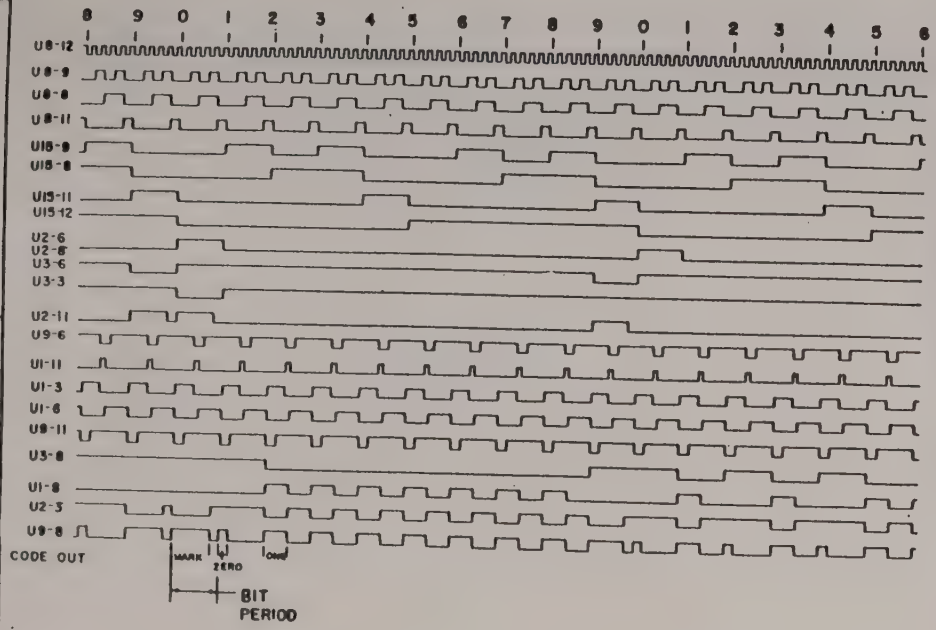
SIZE	CODE IDENT NO.		REV
2	24672	10302554-1	G

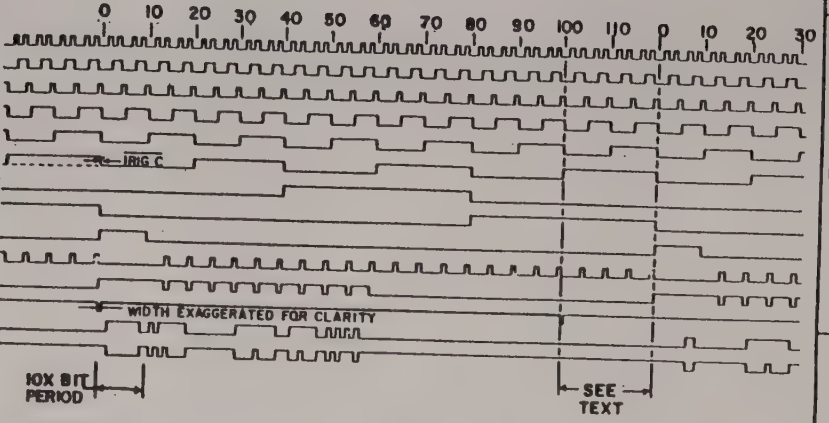
SCALE 2:1 SHEET 1 OF 2

1. STAMP ASSY DASN NO.

NOTE:

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	–	RELEASED	5/4/84	RDB





CODE SHOWN (SERIAL ONES & U18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE

5-29

10302554-1	8155-0457		4-8	TOLERANCES UNLESS OTHERWISE SPECIFIED: DEC / FRAC / ANG	AUSTRON INC. AUSTIN, TEXAS		
NEXT ASSY	USED ON	REF DES	FIG NO.	MATERIAL:	IRIG CODE GENERATOR TIMING DIAGRAM		
APPLICATION DA / Rel / 5-7-84				ENGR RCH 5/4/84	SIZE 2	CODE IDENT NO. 24672	REV 12402554
				CHECK RDB 5/4/84	SCALE		SHEET 1 OF 1
				DRAWN VMy 4/3/84			

ASSEMBLY PCB ASSY CODE GENERATOR
ASSEMBLY NUMBER 10302554-1
REFERENCE DESIGNATOR PREFIX 1A3A22
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010R2	56289
C2	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C3	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 390 OHM 1/4W 10%	651102-0391	RC07GF391K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R3	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R4	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC QUAD 2-IN NOR GATES	703MC1810P	MC1810P	04713
U2	IC QUAD 2-IN NOR GATES	703MC1810P	MC1810P	04713
U3	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U5	IC QUAD 2-IN NOR GATES	703MC1810P	MC1810P	04713
U6	IC QUAD 2-IN NOR GATES	703MC1810P	MC1810P	04713
U7	IC DECADE COUNTER	703SN7490N	SN7490N	01295
U8	IC DECADE COUNTER	703SN7490N	SN7490N	01295
U9	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U16	IC HEX INVERTER	703SN74LS04N	SN74LS04N	01295
U17	IC PRESETABLE BINARY COUNTER/LATCH	703SN74LS197	SN74LS197N	01295
U17	IC DECADE COUNTER	703SN7490N	SN7490N	01295
U18	IC TRIPLE 3-INP NAND GATE	703SN7410N	SN7410N	01295
W1	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210

5.3.5. Shaper/Modulator
(Schematic Dwg. No. 12302556-05)

The Shaper/Modulator PCB can be assembled to provide up to three shaper circuits, a modulator, a dc code output buffer, a Days/ID control circuit, a square wave decoder and miscellaneous inverters and buffers. This shaper circuits are identical with the exception that three capacitors within each circuit are a function of frequency. The following description is intended to apply to all PCB configurations. The specific assembly used is covered by the attached assembly, schematic and parts list.

5.3.5.1. Shapers

Each of the shaper circuits (up to three) are identical, with the exception that the values chosen for three capacitors in each circuit are inversely proportional to the resonant frequency. Each shaper accepts a logic level square wave at the selected carrier frequency and outputs an in-phase sine wave which may be selected (through switching external to the card) and fed to the modulator. The input is filtered and applied to the base of a constant-current amplifier which drives an active circuit having the electrical properties of a tuned tank circuit. A potentiometer is provided to adjust the resonant frequency. The sine wave output from this circuit is buffered and ac-coupled to output pin M, S or T.

5.3.5.2. Modulator

The modulator accepts the selected carrier sine wave at pin W and modulates it with the dc level shift code at pin F. The resulting modulated code is fed through amplifier (U4) to output pin X.

A MODULATED RATIO adjustment, R16, sets the percentage of modulation before the signal is fed to (U4). A MODULATED CODE AMPLITUDE adjustment, R20, determines the gain of amplifier (U4), thus, establishing the signal level at pin X. (0 to $\pm$10 Vp-p.)

5.3.5.3. DC Code Buffer

The dc level shift code input to pin F is inverted once by (U1,11) and again by Q4 before being fed as the dc code output to pin 21, through R25. Transistors Q2 and Q3, and the DC CODE AMPLITUDE potentiometer R23, establish the output level at pin 21 (0.4 Vdc to 10 Vdc). Short-circuit protection is provided by CR3, CR4 and R24. The quiescent current in Q3 and Q4 is determined by CR3, CR5 and R25.

5.3.5.4. DAYS/ID (Run Number) Control

Gates on (U3) control the selection of the signal which is used to update the days accumulator in the system. The carry output from the time-of-day accumulator is inverted and applied to (U3,9). If the other input (the ID NUM line) is high (i.e. left open), the hours accumulator carry will update the days accumulator. Similarly, a high on the DAYS line permits a signal on pin B (ID NUM ADV) to update the days accumulator. The ID advance input pulses are standardized by one-shot (U3,3 and 6) to ensure reliable operation.

5.3.5.5. Square Wave Decoder

This circuit, formed from gates on (U2), generates a square waves from the BCD outputs fed to pins C, D and N from an external decade counter. It consists of a flip-flop (U2,8 and 11) which is ac-set at mid-period when the output from (U2,6) goes to ground (1 and 4 bits both positive). The flip-flop is ac-reset by the trailing edge of the 8 bit. The result is a square wave at (U2,11). The output pulse rate is a function of the source of input signals.

5.3.5.6. Buffers

Extra gates on (U1) and (U2) are made available for external use as inverters and buffers.

	REVISIONS				
B	CIRCUIT CHG. DATES		353		
C	ADDED NOMEN. TO POTS				
D	R24 WAS 33Ω		679		
E	C29 (.01 μf) WAS .001 μf.	-	11673		
F	DWG NO WAS 21556-7-5	-	12837		
G	REVISED PER ECO 6539		16539		

1 KC SHAPER

1KPPS (V) · 1KC SINE (T) · W

R55 47K · R56 560K · Q5 MPF-105 · C23 .22μf 100V · R54 0Ω · C5 .01μf 50V · R57 220K · TUNE R53 1K · R49 68K (NOM) · Q6 2N3565 · R50 56K (NOM) · Q7 MPF-105 · C6 .01μf 50V · C4 .003μf 100V · R51 10K · R52 5.6K · R13 10K · W1 · R15 8.2K · C24 .47μf 35V · R27 2.7K · +15V

Q1 MPF-152 · RATIO R16 5K · R14 10K · C12 1000pf 100V · R17 1M · CR1 · VCC · CODE IN (F) · U1 · W2 · P · R26 560

R18 8.2K · R19 10K · C11 XXX · R20 100K · MOD · R28 10K · U4 · C25 .0022 200V · C3 6.8μf 35V · R21 750 · TP-2 MOD · X · 22 -15V · Z

C2 6.8μf 35V · R22 6.8K · Q2 2N4126 · Q3 2N4124 · CR2 · CR3 · R24 18 · TP-1 DC · 21 DC CODE OUTPUT · R23 10K · DC · C26 .47μf 35V · CR4 · CR5 · R25 120 · Q4 2N4124 · 23 +15V · AA

VCC · C1 39μf 10V · L1 R45-4 · 24 +5V · BB · 25 GRD · CC

R5 10K · R2 100 · Vcc · CR6 70111N4G1C · DATA (A) · I.D. NUM ADV. (B) · C9 .001μf 200V · U3 · R6 3.9K · R9 10K · R11 3.9K · C10 10μf 20V · R10 1K · R7 3.9K · R12 3.9K · C29 .01μf · MRS CNTRY (3) · C28 .001μf · TO TM. (2) · (1) · R8 10K

E · H · K · J · L · U1

NOTE:
1.) PIN 7 U1 & U3 CONNECTED TO GRD.
PIN 14 " " " " " VCC.
2.) RESISTORS — Y&W 5% UNLESS NOTED OTHERWISE
3.) U1 & U3 ARE MC-846.
U4 IS MC1439P.

Q-13
C-29
R-57
CR-6

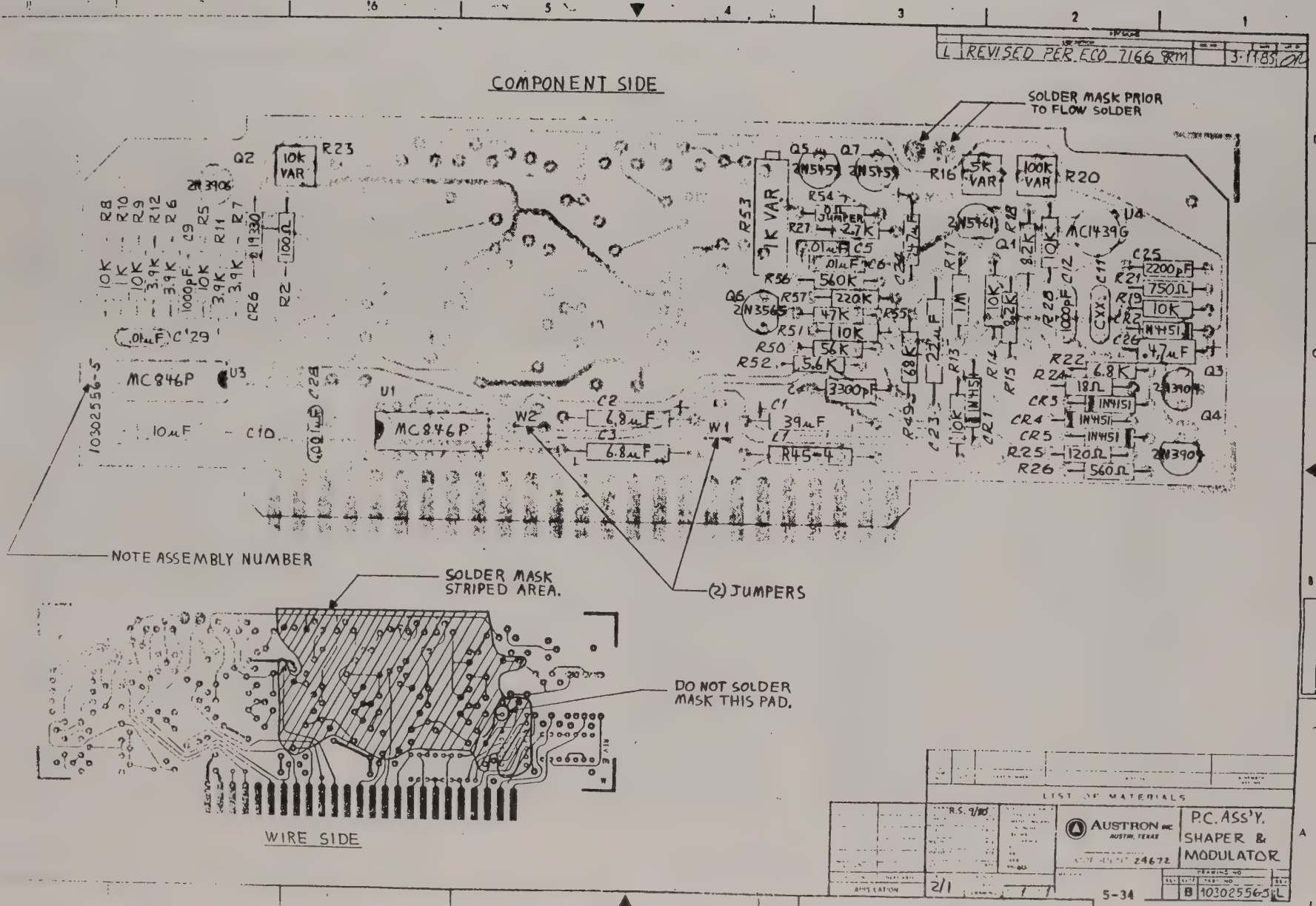
LIST OF MATERIALS

AUSTRON INC. AUSTIN, TEXAS

SCHEMATIC, SHAPER & MODULATOR

123025565 G

5-33


L REVISED PER ECO 7166 RM 3-1185
COMPONENT SIDE
SOLDER MASK PRIOR TO FLOW SOLDER
Q2
2N3906
R23 10k VAR
R8 10K
R10 1K
R9 10K
R12 3.9K
R6 3.9K
R5 1000pF
C9
R11 10K
R7 3.9K
CR6
R2 100Ω
1930Ω
.01μF C29
MC846P U3
10μF C10
.01μF C28
U1
MC846P
W2
C2 6.8μF
C3 6.8μF
W1
C1 39μF
L1 R45-4
Q5 2N5195
Q7 2N5195
R53 1K VAR
R54 0Ω JUMPER
R27 2.7K
.01μF C5
.01μF C6
R56 560K
Q6 2N3565
R57 220K
47K
R55
R51 10K
R50 56K
R52 5.6K
3300pF
68K
2.2μF
R49
C23
R13 1M
R14 10K
R15 8.2K
CR1 IN4151
R16 5K VAR
100K VAR R20
R18 8.2K
10K
Q1
C12
C11
CXX
R23 1000pF
2N5961
U4 MC1439G
C25 2200pF
R21 750Ω
R19 10K
CR2 IN4151
C26 .47μF
R22 6.8K
R24 18Ω
Q3 2N3904
CR3 IN4151
CR4 IN4151
CR5 IN4151
Q4
R25 120Ω
R26 560Ω
2N3904
10302556-5
NOTE ASSEMBLY NUMBER
SOLDER MASK STRIPED AREA.
(2) JUMPERS
DO NOT SOLDER MASK THIS PAD.
WIRE SIDE
LIST OF MATERIALS
AUSTRON INC AUSTIN, TEXAS
P.C. ASS'Y. SHAPER & MODULATOR
24672
B 10302556-5L
2/1
5-34

ASSEMBLY PCB SHAPER & MODULATOR
ASSEMBLY NUMBER 10302556-5
REFERENCE DESIGNATOR PREFIX 1A3A20
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	50V DIO SIG	7011N4151	1N4151	13715
CR2	50V DIO SIG	7011N4151	1N4151	13715
CR3	50V DIO SIG	7011N4151	1N4151	13715
CR4	50V DIO SIG	7011N4151	1N4151	13715
CR5	50V DIO SIG	7011N4151	1N4151	13715
CR6	DIO S ZEN DO-7 2.2 V 250MW 05	7011N4616	1N4616	08288
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	6.8 UF 35V 10 CAP TANT	608017-0685	CS13BF685K	81349
C3	6.8 UF 35V 10 CAP TANT	608017-0685	CS13BF685K	81349
C4	.0033UF 200V 10 CAP MYLAR	604192-0010	192P33292	56289
C5	.01UF 50V 5 POLY-FOIL POTTEDRAD	604315-0103	719D1AA103PJ500AX	99392
C6	.01UF 50V 5 POLY-FOIL POTTEDRAD	604315-0103	719D1AA103PJ500AX	99392
C9	.001 UF 200V 10 CAP MYLAR	604192-0005	19210292	56289
C10	10 UF 20V 10 CAP TANT	608016-0106	CS13BE106K	81349
C12	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C23	.22 UF 100V METMYL	602040-0224	XA2B224K	27556
C24	.47 UF 35V 10 CAP TANT	608017-0474	CS13BF474K	81349
C25	.0022UF 200V 10 CAP MYLAR	604192-0009	192P22292	56289
C26	.47 UF 35V 10 CAP TANT	608017-0474	CS13BF474K	81349
C28	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C29	.01 UF 100V 20 CAP CERAMIC	601004-0103	TG-S10	56289
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
Q1	TO-92 XSTR JFET	7022N5461	2N5461	04713
Q2	0.31W TO-92 XSTR PNPS SH	7022N3906	2N3906	81349
Q3	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q4	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q5	TO-92 XSTR JFET	7022N5459	2N5459	04713
Q6	25V TO-92 XSTR NPNS	702PN3565	PN3565-18	07263
Q7	TO-92 XSTP JFET	7022N5459	2N5459	04713
R2	RES FXD COMP 100 OHM 1/4W 05%	651100-0101	RC07GF101J	81349
R5	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349

ASSEMBLY PCB SHAPER & MODULATOR (CONT)
ASSEMBLY NUMBER 10302556-5
REFERENCE DESIGNATOR PREFIX 1A3A20
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R6	RES FXD COMP 3.9 K 1/4W 05%	651100-0392	RC07GF392J	81349
R7	RES FXD COMP 3.9 K 1/4W 05%	651100-0392	RC07GF392J	81349
R8	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R9	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R10	RES FXD COMP 1 K 1/4W 05%	651100-0102	RC07GF102J	81349
R11	RES FXD COMP 3.9 K 1/4W 05%	651100-0392	RC07GF392J	81349
R12	RES FXD COMP 3.9 K 1/4W 05%	651100-0392	RC07GF392J	81349
R13	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R14	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R15	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R16	RES VAR CERMET 5 K 1/2W 10	659010-0502	82PAR5K	73138
R17	RES FXD COMP 1 M 1/4W 05%	651100-0105	RC07GF105J	81349
R18	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R19	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R20	RES VAR CERMET 100 K 1/2W 10	659010-0104	82PAR100K	73138
R21	RES FXD COMP 750 OHM 1/4W 05%	651100-0751	RC07GF751J	81349
R22	RES FXD COMP 6.8 K 1/4W 05%	651100-0682	RC07GF682J	81349
R23	RES VAR CERMET 10 K 1/2W 10	659010-0103	82PAR10K	73138
R24	RES FXD COMP 18 OHM 1/4W 05%	651100-0180	RC07GF180J	81349
R25	RES FXD COMP 120 OHM 1/4W 05%	651100-0121	RC07GF121J	81349
R26	RES FXD COMP 560 OHM 1/4W 05%	651100-0561	RC07GF561J	81349
R27	RES FXD COMP 2.7 K 1/4W 05%	651100-0272	RC07GF272J	81349
R28	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R49	RES FXD COMP 68 K 1/4W 05%	651100-0683	RC07GF683J	81349
R50	RES FXD COMP 56 K 1/4W 05%	651100-0563	RC07GF563J	81349
R51	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R52	RES FXD COMP 5.6 K 1/4W 05%	651100-0562	RC07GF562J	81349
R53	1 K 3/8W 10 POT 15T PC CERM	659020-0102	89PR1K	73138
R55	RES FXD COMP 47 K 1/4W 05%	651100-0473	RC07GF473J	81349
R56	RES FXD COMP 560 K 1/4W 05%	651100-0564	RC07GF564J	81349
R57	RES FXD COMP 220 K 1/4W 05%	651100-0224	RC07GF224J	81349
U1	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U3	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295

ASSEMBLY PCB SHAPER & MODULATOR (CONT)
ASSEMBLY NUMBER 10302556-5
REFERENCE DESIGNATOR PREFIX 1A3A20
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U4	IC OP AMP	703MC1439G	MC1439G	04713

5.3.6. Time Base/Serial Preset-Reset (Schematic Dwg. No. 12302566-15)

5.3.6.1. Time Base

The Time Base section consists of an unheated crystal, Y1, and feedback amplifier Q1. This oscillator output, at pin Y, may be utilized as an external reference or it may be jumpered to pin W for internal use on the PCB. An external reference signal may be utilized by applying it to pin W in place of the above signal.

The time base signal is applied to the base of voltage-amplifier Q2 (which has a gain of three), isolated, and applied to the base of Q3. Clipper-circuit Q3 provides a 5 Vp-p square wave at pin X.

5.3.6.2. Divider Chain

Control gate (U5,6) receives the output of Q3 (jumper W1 installed) or an input through pin 13 depending upon the time base pulse rate and the application.

The time base pulse rate at this point is usually 1 Mpps. Control gate (U5,6) has two other inputs. One is the Elapsed input from pin 14 and the other is from Stop/Start flip-flop (U4,5).

When a logic ZERO (ground) is applied to the External Stop line (pin T), flip-flop (U4,5) will generate a logic ZERO which will close gate (U5,6) and inhibit the time base input to the divider chain. A positive transition on pin 11 or R, (the Stop time input) will also inhibit the time base if pin S is at ground.

A ground signal on the $\overline{\text{START}}$ pin 12 or P, will clear the inhibit from (U5,6).

The divider chain consists of up to three divider ICs (U12), (U13) and (U6) connected in tandem. In most PCB configuration, these are used as decades. They divide the 1 mpps time base down to 1 kpps. The first two (U12) and (U13) are connected as divide-by-five, then-by-two counters. These develop 100 kpps and 10 kpps square waves at pin 20 and 15, respectively. The third decade (U6) is connected in the normal divide-by-two, then-by-five arrangement. BCD outputs (1-2-4-8) are provided at pins 21, U, V and 17. Flip-flop (U4,9) develops complementary 1 kpps square wave outputs at pins 10 and 9.

Pin 2 is the ZERO reset input to (U12). The ZERO reset input to (U13) and (U6) are connected to pin 19. These two inputs may be jumpered together through W4. These lines must be grounded if not in use.

REVISIONS					
REV	DESCRIPTION		ENG NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS				5/14/81	
A_1	PIN 11 WAS 5, R WAS 11, A1-5 WAS DUP GD. (ECO 8113-81)	(ENG 12681)	NFC		10/20/81	PJH
B	DWG NO. WAS 021566-7-15		4337		8/2/82	
C	REV PER ECO 7627 PJ	-	-		7/85	DR
D	REV PER ECO 8169 PJ	-	-		11/85	DR

+15V
OUT IN
STOP TIME
START
VCC
4X10-6
1X10-6
5X10-6
5X10-5
1X10-4
4X10-4
2X10-4
8X10-4
R1 47
R2 33K
C2 6.8µf 35V
R4 8.2K 1/2W
Q1 2N3904
R3 6.8K
Y1 1MHz
C5 680 pf
C6 300 pf
R5 220
C3 0.8-18pf
C4 22pf
C7 1000 pf
R6 620
R7 12K
Q2 2N3904
R8 1.8K
R9 100
R10 470
C8 1000 pf
CR1 IN 4151
R11 470
Q3 MPS3646
W1
W2
W3
R12 4.7K
R35 10K
W5
W6
W4
U12
U13
U4
U5
U6
R34 10K
R14 4.7K
R13 10K
C9 1000pf
C13 330 pf
R15 6.8K
R16 8.2K
L1 R45-4
+5V
GND
C1 39µf 10V
PRESET
EXT STOP
ELAPSED TIME
RESET A
RESET B
5X10-4
5X10-3

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4W CARB COMP VALUED IN OHMS @ 5%
2. INT CKTS ARE AS FOLLOWS;

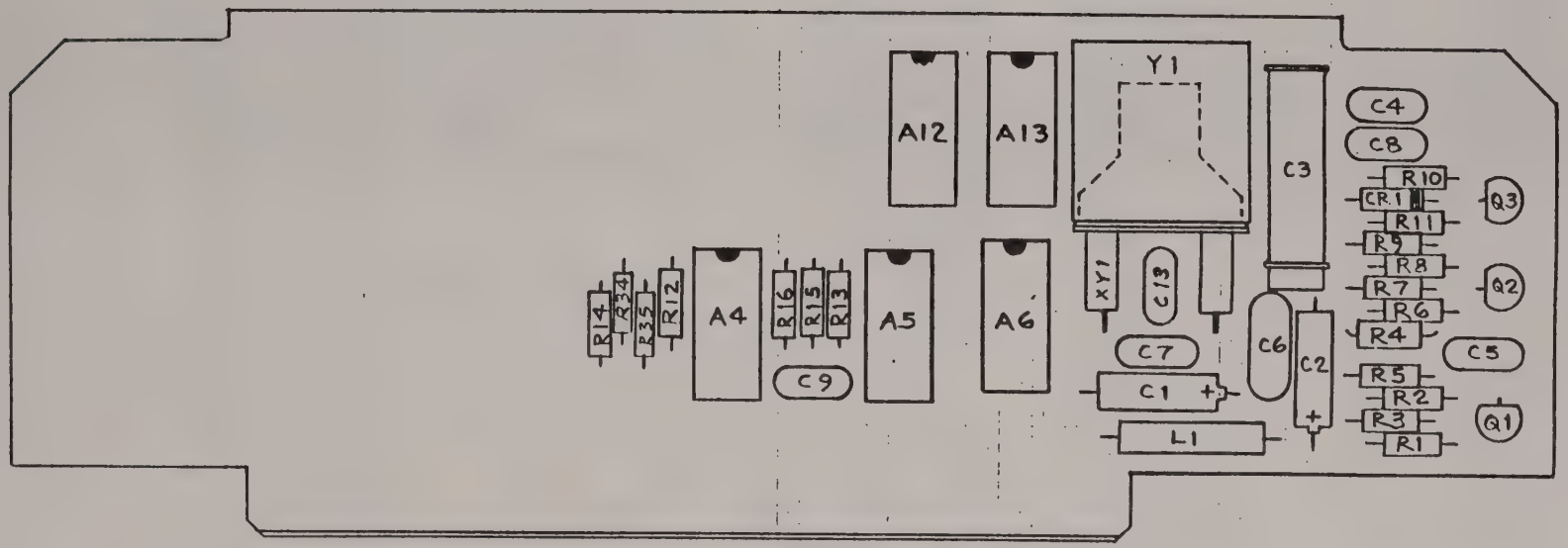
REF	JEDEC NO	TYPE	Vcc	GND
U4	SN7474N	DUAL D FLIP FLOP	14	7
U5	SN7410N	TRI (3 INPUT) NAND GATE	14	7
U6,12,13	SN7490N	DECADE COUNTER	5	10

ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE ± .XX ± .XXX ANGLES ±	AUSTRON AUSTIN, TEXAS
CHECK	DATE		TIME BASE
ELECT	DATE		CODE IDENT 29672
MECH	DATE		DRAWING NO B 12302566-15 REV D
QA	DATE		MATERIAL 5-39
USED ON	NEXT ASSY	DO NOT SCALE DRAWING	SH 1 OF 1
APPLICATION		SCALE —	

REV	DESCRIPTION	BY	DATE	APVD
A	RELEASED TO RECORDS			
A1	ADDED: A12, A13, R12, R14, R34, R35 & (CHANGED)	-	MR	
B	DWG WAS 02-5999-4-15 ECO 4837	ECO 6395		
C	P/L REVISED	[illegible]		
D	REV PER ECO 7623	PJ	-	
E	REV PER ECO 8169	PJ	11-6-85	



LIST OF MATERIALS

ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

DRAWN	1/29/80	AUSTRON INC AUSTIN, TEXAS	P.C. BD. ASSEMBLY
CHECK			
ENGR		CODE IDENT 52542	
MFG			
USED ON / NEXT ASSY	APPLICATION	SCALE 2/1	SHT 1 OF 2
MATERIAL	5-40	DRAWING NO. REF SIZE B	PART NO 103025663 REV E

ASSEMBLY PCB ASSY T.B. SERIAL PRESET/RESET
ASSEMBLY NUMBER 10302566-15
REFERENCE DESIGNATOR PREFIX 1A3A27
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	50V DIO SIG	7011N4151	1N4151	13715
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	6.8 UF 35V 10 CAP TANT	608017-0685	CS13BF685K	81349
C3	CAP VAR PSTN PCMTG .8-18PF Q=500	609525-0001	GGC18000	56289
C4	22 PF 500V 5 CAP DIP MICA	603000-0220	DM15-220J	02799
C5	680 PF 300V 5 CAP DIP MICA	603000-0681	DM15-681J	72136
C6	3000 PF 500V 5 CAP DIP MICA	603000-0302	CD19FD302J03	72136
C7	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C8	1000 PF 100V 5 CAP DIP MICA	603000-0102	CM05FA102J03	81349
C9	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C13	330 PF 500V 5 CAP DIP MICA	603000-0331	DM15-331J	02799
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
MP3	EYELET 3/32DX3/116L BRASS	520105-0015	SE-36	07707
MP4	EYELET 3/32DX3/116L BRASS	520105-0015	SE-36	07707
Q1	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q2	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q3	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
R1	RES FXD COMP 47 OHM 1/4W 05%	651100-0470	RC07GF470J	81349
R2	RES FXD COMP 39 K 1/4W 05%	651100-0393	RC07GF393J	81349
R3	RES FXD COMP 6.8 K 1/4W 05%	651100-0682	RC07GF682J	81349
R4	RES FXD COMP 820 OHM 1/2W 10%	651103-0821	RC20GF821K	81349
R5	RES FXD COMP 220 OHM 1/4W 05%	651100-0221	RC07GF221J	81349
R6	RES FXD COMP 1.2 K 1/4W 05%	651100-0122	RC07GF122J	81349
R7	RES FXD COMP 47 K 1/4W 05%	651100-0473	RC07GF473J	81349
R8	RES FXD COMP 12 K 1/4W 05%	651100-0123	RC07GF123J	81349
R9	RES FXD COMP 390 OHM 1/4W 05%	651100-0391	RC07GF391J	81349
R10	RES FXD COMP 1 K 1/4W 05%	651100-0102	RC07GF102J	81349
R11	RES FXD COMP 2.7 K 1/4W 05%	651100-0272	RC07GF272J	81349
R12	RES FXD COMP 4.7 K 1/4W 05%	651100-0472	RC07GF472J	81349
R13	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R14	RES FXD COMP 4.7 K 1/4W 05%	651100-0472	RC07GF472J	81349

ASSEMBLY PCB ASSY T.B. SERIAL PRESET/RESET (CONT)
ASSEMBLY NUMBER 10302566-15
REFERENCE DESIGNATOR PREFIX 1A3A27
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R15	RES FXD COMP 6.8 K 1/4W 05%	651100-0682	RC07GF682J	81349
R16	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R34	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
R35	RES FXD COMP 10 K 1/4W 05%	651100-0103	RC07GF103J	81349
U4	IC DUAL D-TYPE POS-EDGE-TRIG FF	703SN7474N	SN7474N	01295
U5	IC TRIPLE 3-INP NAND GATE	703SN7410N	SN7410N	01295
U6	IC DECADE COUNTER	703SN7490N	SN7490N	01295
U12	IC DECADE COUNTER	703SN7490N	SN7490N	01295
U13	IC DECADE COUNTER	703SN7490N	SN7490N	01295
XY1	SOCKET, XTAL MTG	551016-0006	M12883-39-01	91506
Y1	XTAL 1.000000 MHZ	75281000000	CR18/U	00000

5.3.7. Power Supply
(Schematic Dwg. No. 12304810-09)

The power supply provides four, regulated dc voltages (±5 Vdc and ±15 Vdc); five unregulated dc voltages (±9 Vdc, ±21 Vdc and 210 Vdc), and an 18 Vrms time base output at the line frequency. The regulated output voltage levels are adjustable. These outputs are current limited and are short-circuit-proof to ground. Both voltage-sense and sense-return lines are provided for the regulated outputs. These lines are wired to provide regulation at the load. Fuses are provided for the unregulated 21 Vdc and 210 Vdc on the power supply assembly.

CAUTION

A short-circuit condition maintained over an extended period of time results in overheating.

Input power is 115/230 Vac, 48 Hz to 440 Hz at less than 100 W with nominal ac line voltage and all outputs fully loaded. Input power is fed to transformer T1 through line filter Z1, fuse F1, a front panel power switch and 115/230 Vac select switch, S101. The third wire is grounded to the chassis.

The transformer is constructed with split-primary windings which are connected in parallel for 115 Vac operation and in series for 230 Vac operation. Selection is made by 115/230 Vac switch, S101. (Note: Units are normally shipped in the 115 Vac configuration with a 2A Slo-Blo fuse, F1. If the unit is converted to 230 Vac operation, F1 should be changed to 1A Slo-Blo.) Three secondary windings (two with center taps) are provided, one for ±9 Vdc, one for ±21 Vdc and 18 Vrms, and the third for 210 Vdc.

5.3.7.1. Nonregulated Supply Circuits

The 210 Vdc nonregulated supply is developed by the bridge rectifier formed from diodes CR5 through CR8, plus the filter circuit formed from R1, R2 and C5. The resulting output is fed through F2 (0.125A) to XA101, pins 18 and V. It is used to drive front panel numerical indicating tubes and is rated at 100 mA.

The ±21 Vdc nonregulated supplies are developed by bridge rectifier CR1 through CR4 and filtered by C1, C2, C8 and C11. The 21 Vdc output is used internally as the source for the 15 Vdc regulator. It is fed through F3 (1A) to XA101, pins 15 and S, where it is available for use as a relay supply. The -21 Vdc output is used internally as the source for the -15 Vdc regulator, and to power both the -15 Vdc and -5 Vdc regulator amplifiers. It is also available at XA101, pin 4, for external use. Each of the ±21 Vdc supplies is rate at 0.5A.

The 18 Vrms is derived from the secondary winding which provides the ac voltage to develop the ±21 Vdc. This rms voltage is fed through R15 to XA101, pins 22 and Z.

The 9 Vdc nonregulated supply is developed by full-wave rectifier CR11, CR12 and filtered by C3, C4 and C10. It is used internally as the source for the 5 Vdc regulator, and to power both the -15 Vdc and -5 Vdc regulator amplifiers. It is available at XA101, pins 21 and Y, for external use as a lamp supply. It is rated at 4A.

The -9 Vdc nonregulated supply from full-wave rectifier CR9, CR10 and filter C6 is used internally as the source for the -5 Vdc regulator. It is available at XA101, pin 2, for external use. It is rated 0.5A.

5.3.7.2. Regulated Supply Circuits

The regulated 15 Vdc, 0.5A output at XA101, pin N, is established through pass transistor Q1 under the control of regulator U1 and the divider network (R4, R5, R6) between the 15 Vdc SENSE line (XA101, pin 12) and ground. The voltage on the arm of 15 Vdc ADJ potentiometer (R5) is fed to U1 where it is compared with the internal reference, referred to the ±15 Vdc sense-return line (XA101, pin 8). The current limit is imposed by sensing the drop across R9 approaches 0.34 Vdc and this circuit is stabilized by network R32, C7.

The regulated -15 Vdc, 0.5A output at XA101, pin E, is established through Q2 and Q3 under the control of regulator amplifier (U3,12). It uses the 15 Vdc SENSE line as the reference, comparing it with the output through R10, R11 and the -15 Vdc supply. Potentiometer R5 serves as the adjustment for both outputs. Current is limited by cutting the base drive to Q2 when the drop across R14 approaches 0.34 Vdc.

The regulated 5 Vdc, 4A output at XA101, pins P and R, is established through Q4 and Q5 under the control of regulator (U2) and a divider network (R18, R19). The 5 Vdc SENSE line at XA101, pins 13 and 14, is compared with the fraction of the U2 internal reference voltage appearing on the arm of 5 Vdc ADJ potentiometer (R19). The current limit is imposed by sensing the drop across R24 approaches 0.4 Vdc through divider (R22, R23). The circuit is stabilized by network (R33, C12). The regulated -5 Vdc, 0.5A output at XA101, pin C, is established through Q6 and Q7 under the control of regulator amplifier (U3,10). It uses the 5 Vdc SENSE line as reference, comparing it with the output through R26, R27 and the -5 Vdc SENSE line at XA101, pin 3. The -5 Vdc output tracks the 5 Vdc supply and potentiometer R19 adjusts both. Output current is limited by cutting the base drive to Q6 when the drop across R30 approaches 0.34 Vdc.

5.3.7.3. Power Supply Calibration Procedure

Test Equipment: see Section Four, Table 4-1.

Check that fuse F1 is the proper size for the input voltage selected:

Fuse	Amperes	Voltage
2	A	115 Vac
1	A	230 Vac

With an input of 115 Vac (230 Vac if so equipped) ±5 percent, 50 to 60 Hz, check the following at the Power Supply PCB edge-connector, P103.

Table. 5-14: Power Supply Voltage Checks.

	Volts	Pin	Ground
1.	210 V ±25 percent	at pins V, 18	(GND 20, X)
2.	21 V ±20 percent	at pins S, 15	(GND BLACK TEST POINT)
3.	9 V ±20 percent	at pins Y, 21	(GND BLACK TEST POINT)
4.	-9 V ±20 percent	at pin 2	(GND BLACK TEST POINT)
5.	-21 V ±20 percent	at pin 4	(GND BLACK TEST POINT)

Table. 5-15: Power Supply Adjustments.

	Voltage	Test Point	Ground	Adjust
1.	15 Vdc ±0.3	BLUE	BLACK	R5 (15 Vdc ADJ)
2.	-15 Vdc ±0.3	VIOLET	BLACK	R5 (15 Vdc ADJ)
3.	5 Vdc ±0.3	RED	BLACK	R19 (5 Vdc ADJ)
4.	-5 Vdc ±0.3	GREEN	BLACK	R19)5 Vdc ADJ)

REV. CONT.				
G	REVISED P.C.B. ECO 9035		9035	

REVISIONS				
DWG	DESCRIPTION	ENG. INIT.	ECO NO.	DATE
A	NEW 5VD. POWER SUPPLY			
B	C3,4,C6 WERE 4500 μf		11251	
C	DELETED J201, CORRECTED NOTES 1 & 3.	-	11355	
C1	ADDED TP REF NOS		NFC	
D	DWG NO WAS 12810-7-5		4337	
E	ADDED C17		6237	
F	ADD POLARITY FOR C17		6460	

18V RMS · UNREG +21V · +15V, +5V, -5V, -15V RETURNS · CHASSIS GND

TP1 BLACK

T1

FAN (REF ONLY) · P102 TYP · J102 TYP

S101 · 115V · 230V

SWITCH (REF ONLY)

J101 115/230 VAC 45-440 Hz · F1 S.L.O.-B.U. 2A 115V 1A 230V · LINE FILTER

R15 1.5K · F3 1A S.B. · C1 2700μf 25V · C2 2700μf 25V · C8 .05μf

CR1 CR2 CR3 CR4

R4 4.7K ½W · R5 5K 15V ADJ · R6 4.7K ½W · R3 3.3K

U1 · 7.2V REF · 6.2V · N.C.

R32 220Ω · C7 .001μf

Q1 2N3766 · R7 1K · R9 0.68 2W, WW · R8 1K

CR10 CR11 MR1120R · CR9 CR12 MR1120R · C3 1300μf 15V · C4 1300μf 15V · C6 680μf 15V

CR5 CR6 CR7 CR8 · R1 390 1W · R2 220K, ½W · C5 95μf 350V · F2 .125A · W1

R18 4.7K ½W 5V ADJ · R19 5K · R20 1.5K

U2 · 7.2V REF · 6.2V · N.C.

R33 220Ω · C12 .001μf · C13 .05μf · C14 .05μf

Q4 2N3766 · Q5 40251 · R21 100 · R22 1K · R24 0.10 5W · R23 3.3K · R25 100 1W

R10 10K 1%, MF · R12 4.7K · C10 .05μf

U3

C15 .05μf · R13 1K · R34 39 · Q3 2N3766 · Q2 2N2905 · CR13 IN4829 · R14 0.68 2W, WW · C17 25μf · R17 1K 1W · CR15 · R16 1K 1W · CR14

R11 10K 1%, MF TP5 VIOLET · C9 .05μf · TP4 BLUE

C11 .05μf · R29 1K · R35 39 · Q7 2N3766 · C16 .001μf · Q6 2N2905 · CR16 IN4829 · R30 0.68 2W, WW · R31 330 1W · CR17

R28 4.7K · R26 10K 1%, MF · R27 10K 1%, MF · TP3 GREEN

TP2 RED

P.C. ASSY POWER SUPPLY BD. 10304804-9

20 X	210V RETURN	13 14	+5V SENSE
18 V	+210V	7	+5V & -5V SENSE RETURN
21 Y	UNREG +9V	P R	REG. +5V
		4	UNREG -21V
		E	REG -15V
		N	REG +15V
		12	+15V SENSE
		B	+15V / -15V SENSE RETURN
		S	-15V SENSE
		2	UNREG -9V
		C	REG -5V
		3	-5V SENSE

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENTS OUTSIDE DOTTED AREA ARE PART OF AC CHASSIS ASSY 11904813-9.
2. ○ INDICATES NUMBERED PAD ON PC ASSY 10304804-9.
3. □ INDICATES PIN NUMBER OF XA101 EDGE CONNECTOR ON PC ASSY 10304804-9.
4. ◎ INDICATES TEST POINT.
5. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
6. ALL CAPACITORS ABOVE 1μf ARE ALUM. ELECTROLYTIC, CAPACITORS BELOW 1μf ARE CERAMIC DISC.
7. ALL DIODES ARE IN4005 (IN5395).
8. U1 & U2 ARE μA723PC. U3 IS μA747PC.

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	8155-0457				
	8150A				
	8130A				
	8120A				
NEXT ASSY	USED ON	REF DES	PIC NO		
APPLICATION					

TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMALS · FRACTIONS · ANGLES

MATERIAL:

ENGR	S.P.A.	2/15/73
CHECKED		
DRAWN	HG	11/24/73

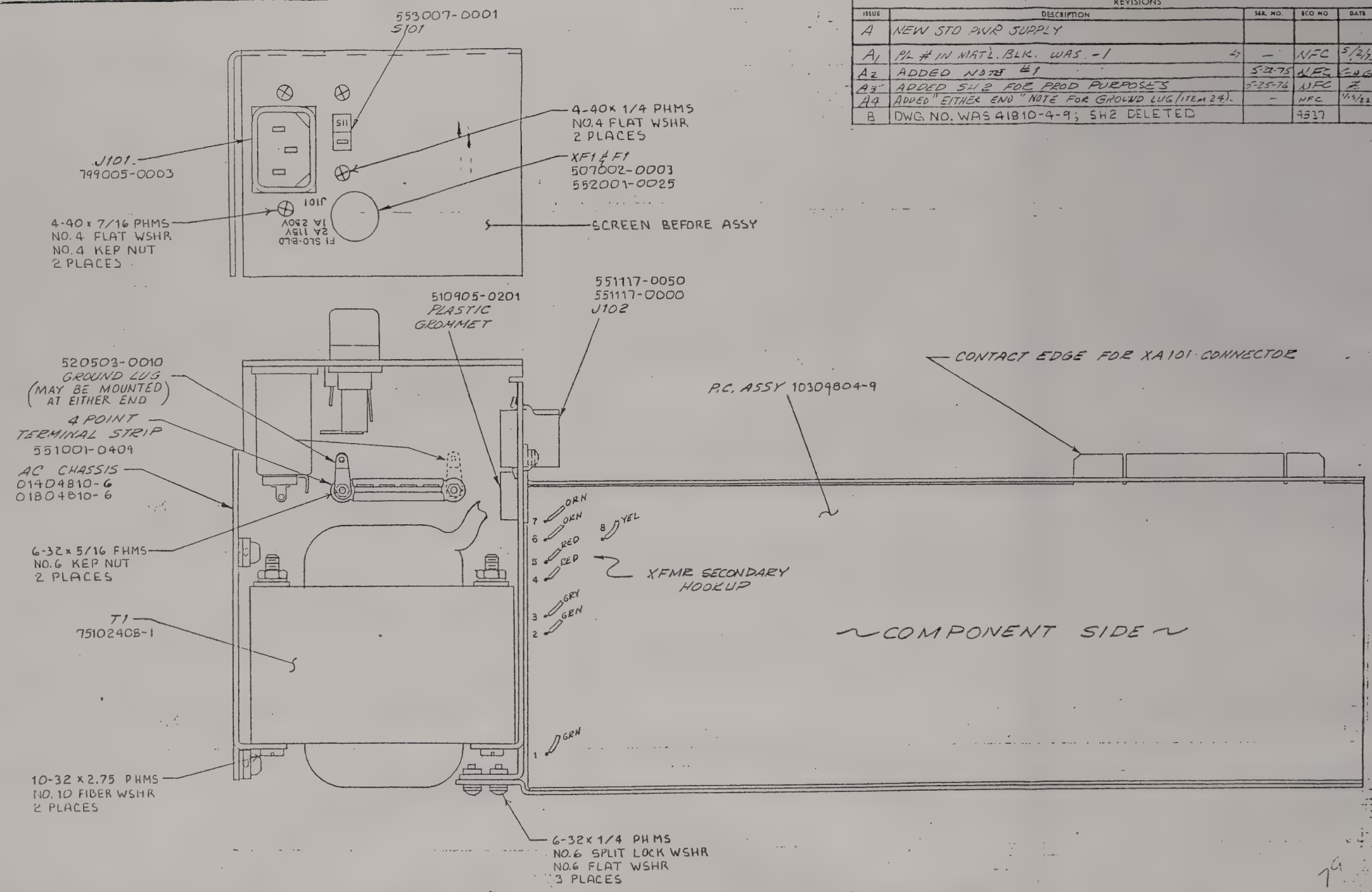
AUSTRON INC. AUSTIN, TEXAS

SCHEMATIC, POWER SUPPLY

SIZE	CODE IDENT NO.		
4	24672	12304810-9	G

SCALE — · SHEET 1 OF 1

REVISIONS					
ISSUE	DESCRIPTION	SER. NO.	ECO NO	DATE	APP BY
A	NEW STD PWR SUPPLY				SKA
A_1	P/L # IN MAT'L. BLK. WAS. -1	—	NFC	5/2/75	LT
A_2	ADDED NOTE #7	5-27-75	NFC	5-29-75	[illegible]
A_3	ADDED SH 2 FOR PROD PURPOSES	5-25-76	NFC	[illegible]	[illegible]
A_4	ADDED "EITHER END" NOTE FOR GROUND LUG (ITEM 24).	—	NFC	11/1/82	BJL
B	DWG. NO. WAS 41810-4-9; SH2 DELETED		9537		



ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO.

LIST OF MATERIALS

8154A	
8130A	
8150A	
USED ON	NEXT ASSY
APPLICATION	

DRAWN [illegible] 2-72 DATE
CHECK LT DATE
ELECT. SA DATE
MECH LT DATE
PROJECT [illegible] 12 NOV 73 DATE
APPROVAL N/A DATE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
X
XX
XXX
ANGLES ±

SCALE 1/1
DO NOT SCALE DRAWING
DWG SIZE C
SH 1 OF 1

AUSTRON INC.
AUSTIN, TEXAS
CODE IDENT. 24672
MATERIAL

POWER SUPPLY ASSEMBLY
DWG NO 23409B10-9
ISSUE B

1. SLEEVING READ ON LINE FILTER, FUSE POST, AND POWER SWITCH WIRING.

ASSEMBLY ASSY POWER SUPPLY
ASSEMBLY NUMBER 23604810-9
REFERENCE DESIGNATOR PREFIX 1A3A101
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PCB ASSY, POWER SUPPLY BOARD	10304804-9		24672
XF1	MIN FUSEHOLDER,R/ANGLE 20AMP S-250V	507002-0003	342004	75915
TB1	TERM STRIP 4TERM 5/16 CM	551001-0404	#2004	52458
J102	HOUSING, RECEPTACLE 5 POS	551117-0000	03-06-1055	27264
P1	PIN MINI FEMALE	551117-0050	02-06-1103	27264
P2	PIN MINI FEMALE	551117-0050	02-06-1103	27264
P3	PIN MINI FEMALE	551117-0050	02-06-1103	27264
P4	PIN MINI FEMALE	551117-0050	02-06-1103	27264
P5	PIN MINI FEMALE	551117-0050	02-06-1103	27264
F1	FUSE 3AG 2 AMP 125V SLO BLO	552001-0025	313002	75915
S101	SW, SLIDE DPDT 115/230V EXC BUSSD	553007-0001	46256LFR	82389
T1	POWER TRANSFORMER	75102408-1		24672
J101	FILTER LINE 3 AMP 115V-230V	799005-0003	3EF1	05245

REVISIONS				
N	PL REVISED PER ECO 7337	-		DL

A	NEW STD.			SRA
A_1	REVISED J201 (INSIDE CONN)	~	NFC	
A_2	ADDED S112 FOR PROD PURPOSES	—	NFC	
B	ADDED V. VALS TO TP'S & POTS	—	NFC	
C	MOVED RED & BLU TEST POINTS.	-		
C_1	SHT 2: ADDED NOTE 1 & ITEM #'s			
J	DWG NO. WAS A1804-4-9 ADDED C17			
K	ADD POLARITY TO C17.			
L	REVISED PER ECO 9035			DL
M	REVISED PER ECO 7267			DL

USE SHOULDER WASHERS TO SPACE HEATSINK OFF P.C. BOARD - SEE DETAIL "A"

REAR ANGLE

FRONT ANGLE

MOUNT Q2 & Q6 WITH PADS — SEE DETAIL "B"

HEAT SINK

SHOULDER WASHER 12 PLCS

P.C. BOARD.

DETAIL "A"

3/8 MAX.

Q2

Q6

DETAIL "B"

NOTES: SEE SHEET 3

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B100A			AUSTRON AUSTIN, TEXAS CODE IDENT 24672	POWER SUPPLY BOARD 10304BC49 P

ASSEMBLY PCB ASSY, POWER SUPPLY BOARD
ASSEMBLY NUMBER 10304804-9
REFERENCE DESIGNATOR PREFIX 1A3A101A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR2	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR3	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR4	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR5	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR6	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR7	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR8	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR9	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR10	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR11	50 V 12A DIO REC	701MR1120	MR1120R	04713
CR12	50 V 12A DIO REC	701MR1120	MR1120R	04713
CR13	20V 1.87V FWD DIO SIG	7011N4829	1N4829	03508
CR14	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR15	400V 1.5A DIO REC	7011N5395	1N5395	04713
CR16	20V 1.87V FWD DIO SIG	7011N4829	1N4829	03508
CR17	400V 1.5A DIO REC	7011N5395	1N5395	04713
C1	2700 UF 25V CAP ELECTROLYTIC	602036-0278	36D272G025AA2A	56289
C2	2700 UF 25V CAP ELECTROLYTIC	602036-0278	36D272G025AA2A	56289
C3	13000UF 15V CAP ELECTROLYTIC	602039-0041	3110-BA133U015AM	99392
C4	13000UF 15V CAP ELECTROLYTIC	602039-0041	3110-BA133U015AM	99392
C5	95 UF 350V CAP ELECTROLYTIC	602039-0950	36D950F350AA2A	56289
C6	680MF 15V CAP ELECTROLYTIC	602003-0681	3070K681T0165F	99392
C7	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C8	.05 UF 50V DISC CERAMIC	601009-0503	TGS50	91418
C9	.05 UF 50V DISC CERAMIC	601009-0503	TGS50	91418
C10	.05 UF 50V DISC CERAMIC	601009-0503	TGS50	91418
C11	.05 UF 50V DISC CERAMIC	601009-0503	TGS50	91418
C12	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C13	.05 UF 50V DISC CERAMIC	601009-0503	TGS50	91418
C14	.05 UF 50V DISC CERAMIC	601009-0503	TGS50	91418
C15	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C16	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289

ASSEMBLY PCB ASSY, POWER SUPPLY BOARD (CONT)
ASSEMBLY NUMBER 10304804-9
REFERENCE DESIGNATOR PREFIX 1A3A101A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
F2	FUSE 3 AG 1/8 AMP	552001-0009	312.125	75915
F3	FUSE 3AGSB 1 AMP 250V	552001-0020	313001	75915
MP1	HEATSINK TRANSISTOR	02004805-1		24672
Q1	20W TO-66 XSTR NPNS	7022N3766	2N3766	04713
Q2	3.0 W TO-5 XSTR PNPS SH	7022N2905	2N2905	08288
Q2MP1	PAD, TSTR MTG, TO-5 CAN	520641-0001	7717-3N	13103
Q3	20W TO-66 XSTR NPNS	7022N3766	2N3766	04713
Q4	20W TO-66 XSTR NPNS	7022N3766	2N3766	04713
Q5	117W TO-3 XSTR NPNS	70240251	40251	02735
Q6	3.0 W TO-5 XSTR PNPS SH	7022N2905	2N2905	08288
Q6MP1	PAD, TSTR MTG, TO-5 CAN	520641-0001	7717-3N	13103
Q7	20W TO-66 XSTR NPNS	7022N3766	2N3766	04713
R1	RES FXD COMP 390 OHM 1W 10%	651104-0391	RC32GF391K	81349
R2	RES FXD COMP 220 K 1/2W 10%	651103-0224	RC20GF224K	81349
R3	RES FXD COMP 3.3 K 1/4W 10%	651102-0332	RC07GF332K	81349
R4	RES FXD COMP 4.7 K 1/2W 10%	651103-0472	RC20GF472K	81349
R5	5 K 1/2W 20 POT 1T PC CERM	659009-1502	3329H-1-502	80294
R6	RES FXD COMP 4.7 K 1/2W 10%	651103-0472	RC20GF472K	81349
R7	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R8	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R9	.68 2 W 5 RES FXD W.W.	652243-0068	BWH.68/2W/5	75042
R10	10 K 1/8W 1 RES FXD FILM	653001-1002	CT410K1%	24546
R11	10 K 1/8W 1 RES FXD FILM	653001-1002	CT410K1%	24546
R12	RES FXD COMP 4.7 K 1/4W 10%	651102-0472	RC07GF472K	81349
R13	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R14	.68 2 W 5 RES FXD W.W.	652243-0068	BWH.68/2W/5	75042
R15	RES FXD COMP 1.5 K 1/4W 10%	651102-0152	RC07GF152K	81349
R16	RES FXD COMP 1 K 1W 10%	651104-0102	RC32GF102K	81349
R17	RES FXD COMP 1 K 1W 10%	651104-0102	RC32GF102K	81349
R18	RES FXD COMP 4.7 K 1/2W 10%	651103-0472	RC20GF472K	81349
R19	5 K 1/2W 20 POT 1T PC CERM	659009-1502	3329H-1-502	80294
R20	RES FXD COMP 1.5 K 1/4W 10%	651102-0152	RC07GF152K	81349
R21	RES FXD COMP 100 OHM 1/4W 10%	651102-0101	RC07GF101K	81349

ASSEMBLY PCB ASSY, POWER SUPPLY BOARD (CONT)
ASSEMBLY NUMBER 10304804-9
REFERENCE DESIGNATOR PREFIX 1A3A101A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
R22	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R23	RES FXD COMP 3.3 K 1/4W 10%	651102-0332	RC07GF332K	81349
R24	0.1 OHM 5W 1 RES FXD W.W.	652019-9010	RE60GR100	91637
R25	RES FXD COMP 100 OHM 1W 10%	651104-0101	RC32GF101K	81349
R26	10 K 1/8W 1 RES FXD FILM	653001-1002	CT410K1%	24546
R27	10 K 1/8W 1 RES FXD FILM	653001-1002	CT410K1%	24546
R28	RES FXD COMP 4.7 K 1/4W 10%	651102-0472	RC07GF472K	81349
R29	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R30	.68 2 W 5 RES FXD W.W.	652243-0068	BWH.68/2W/5	75042
R31	RES FXD COMP 330 OHM 1W 10%	651104-0331	RC32GF331K	81349
R32	RES FXD COMP 220 OHM 1/4W 10%	651102-0221	RC07GF221K	81349
R33	RES FXD COMP 220 OHM 1/4W 10%	651102-0221	RC07GF221K	81349
R34	RES FXD COMP 39 OHM 1/4W 10%	651102-0390	RC07GF390K	81349
R35	RES FXD COMP 39 OHM 1/4W 10%	651102-0390	RC07GF390K	81349
TP1	TESTPOINT, PC, BLK RIGHT ANGLE	551112-0009	105-0853-001	74970
TP2	TESTPOINT, PC, RED RIGHT ANGLE	551112-0010	105-0852-001	74970
TP3	TESTPOINT, PC, GRN RIGHT ANGLE	551112-0008	105-0854-001	74970
TP4	TESTPOINT, PC, BLU RIGHT ANGLE	551112-0007	105-0860-001	74970
TP5	TESTPOINT, PC, VIO RIGHT ANGLE	551112-0011	105-0862-001	74970
U1	IC VOLTREG 2-37V .15A DIP	703LM723CN	LM723CN	27014
U2	IC VOLTREG 2-37V .15A DIP	703LM723CN	LM723CN	27014
U3	OP AMP DUAL AMP	703UA747	UA747	52542
XF2-1	CLIP FUSE .25D PC/MT	552007-0010	102074	75915
XF2-2	CLIP FUSE .25D PC/MT	552007-0010	102074	75915
XF3-1	CLIP FUSE .25D PC/MT	552007-0010	102074	75915
XF3-2	CLIP FUSE .25D PC/MT	552007-0010	102074	75915
XU1	SOCKET, IC 14 PIN DIP, CLOSED ENT	551016-0000	IC-314-SGT	55322
XU2	SOCKET, IC 14 PIN DIP, CLOSED ENT	551016-0000	IC-314-SGT	55322
XU3	SOCKET, IC 14 PIN DIP, CLOSED ENT	551016-0000	IC-314-SGT	55322

5.3.8. Display Assembly
(Schematic Dwg. No. 12304945-02)

The basic display assembly has three 2-digit, in-line, planar indicator tubes and associated driver chips for the display of time in hours, minutes and seconds. LED colons are provided between the tubes. The assembly includes provision for the addition of a three-digit days displayed plus a third colon when Days Option (E13) is added. Time information is accepted in parallel BCD form. A voltage regulator is used to develop 180 Vdc from the 210 Vdc input for use by the display tubes.

The assembly (P/N 12004945-02), is formed from two main subassemblies plus the voltage regulator as shown on the schematic. The Readout PCB Assembly, (P/N 10304766-01), mounts the display tubes and LED colons. The Driver Board Assembly, (P/N 10304772-01), mounts the display drivers which convert the BCD input to the seven segment lines required by the display tubes. The two boards are interconnected by right-angle pin assemblies.

A	REVISED MSR READOUT REDESIGN			11/72	JM
B	READOUT BD, ADD R7-R10; DRIVER, DELETE R4, ADD W5			12/72	JM
C	DELETED R1, R3 & R5 150Ω. R2, R4& R6 WERE 180Ω, DELETE W5		509	1/72	JM
D	ADD Q1, VR1, CR7 (NEW STD.)		11049	7/74	SA
E	REVISED G REF CIRCUIT NOTE NO.		11195	10/74	CAM
E1	R1 THRU R9 WAS 12K		NFC	3/75	V.A.
F	ON 41760-9-1: REVISED FIG. 2 & 3. REVERSED CR1-6.	—	11259	8/1975	C. V.A.
G	Q1 CR7, VR1 MOVED FROM ELECT. INTG TO 41772-9-1.	—	11492	5/76	C. MM.
G1	CHANGED NOTE #3 FROM DS8680		NFC	5/5/76	J. M.
H	ON 41766-9-1: R2, R9, R6 WERE 120; DIODES WERE FLY-ING.	—	17621	7/1/81	L. Hp.
J	DRAWING NUMBER WAS 09995-7-2		18537		

P/O 10304772-1

+210 V

CR7 IN5297 1mA

Q1 2N3400 +180V PIN 1

VR1 IN991B +210V RET PIN 3

READOUT BD. 10304766-1

DAYS

HOURS

MINUTES

SECONDS

R10 4.7K

R9 4.7K

R8 4.7K

R7 4.7K

R6 330

R4 330

R2 330

CR6 CR5 CR4 CR3 CR2 CR1

V4C V4B V4A V3B V3A V2B V2A V1B V1A

C9 B9 A9

U9 U8 U7 U6 U6 U4 U3 U2 U1

R9 10K R8 10K R7 10K R6 10K R5 10K R4 10K R3 10K R2 10K R1 10K

W3 W4 W2 W1

DRIVER BD 10304772-1

10D 1D 1D 10H 1H 10M 1M 10S 1S

+5V +5V RET +210V RET +180V +210V

NOTE: THIS SECTION NOT USED FOR UNITS WITHOUT DAYS

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
2. ALL DIODES ARE H.P. 5082-4480.
3. ALL IC's ARE DS8680N.

ITEM NO	QTY	PART NUMBER	DESCRIPTION	REFERENCE DESIGNATION

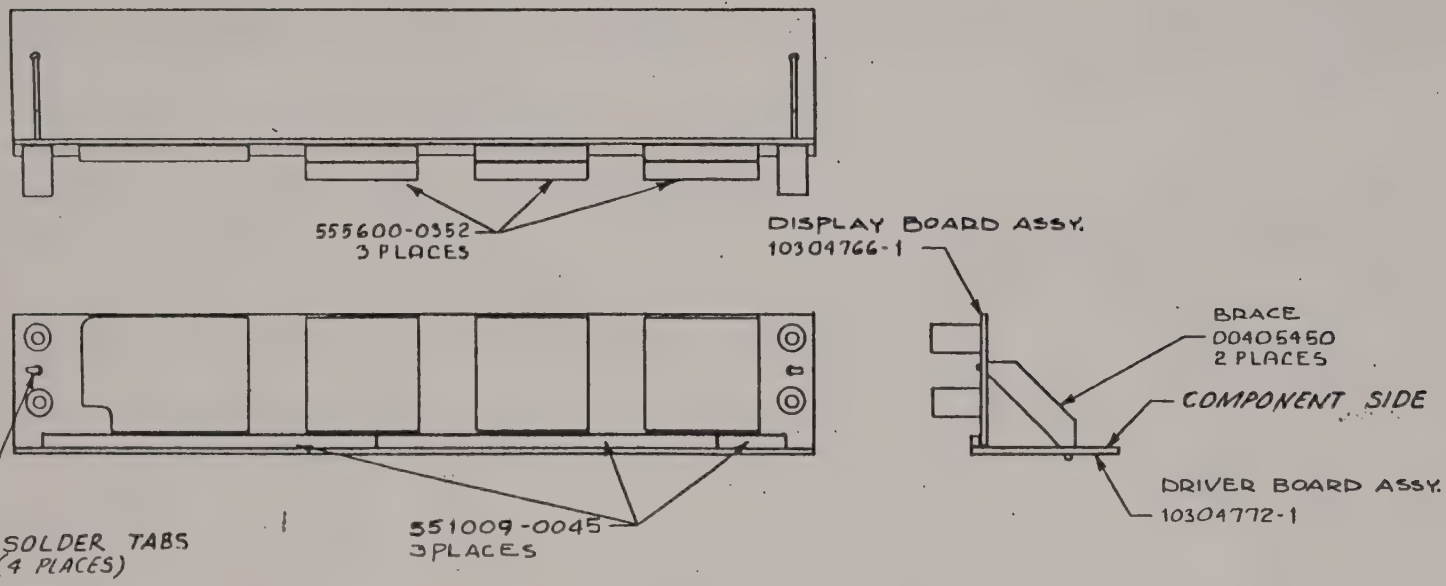
LIST OF MATERIALS

DRAWN	DATE 7/11	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	AUSTRON AUSTIN, TEXAS
CHECK	DATE	DECIMAL TOLERANCE	CODE IDENT. 29672
ELECT. N/A	DATE	.X ±	
MECH. N/A	DATE	.XX ±	
PROJECT.	DATE	.XXX ±	
APPROVAL	DATE	ANGLES ±	
E100A SERIES	SCALE	DO NOT SCALE DRAWING	DWG SIZE D
USED ON	NEXT ASSY		MATERIAL
APPLICATION			

SCHEMATIC, READOUT AND DRIVER

DWG NO 12304945-2 ISSUE J

REVISIONS					
REV	DESCRIPTION	NOTE NO	ECO NO	DATE	APP
E	REDRAWN W/O BRACKET W/COMPONENTS.	-	1140	9/1/77	
E1	"SOLDER TABS" WAS 'BEND & SOLDER'.	-	NFC	9/28	
F	DWG NO. WAS 41995-4-2	—	7357		
G	REVISED PER ECO		7177		



5-55

LIST OF MATERIALS

DRAWN	3/10/77	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE ±	AUSTRON INC AUSTIN, TEXAS	DISPLAY ASSEMBLY, 6 DIGIT
CHECK		DATE			
ELEC		DATE			
MECH		DATE		CODE IDENT 24612	
APPD	5/17/77	DATE	ANGLES ±		
Q+		DATE			
MFG		DATE			
WEIGHT	SCALE				

ASSEMBLY ASSY DISPLAY 6 DIGIT
ASSEMBLY NUMBER 12004945-2
REFERENCE DESIGNATOR PREFIX 1A3A102
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A1	PCB ASSY READOUT,STD 9 DIGIT DIS.	10304766-1		24672
A2	PCB ASSY DRIVERS, STD 9 DIGIT DIS.	10304772-1		24672
MP1	BRKT DISPLAY & DRIVER BD	00405450		24672
MP2	BRKT DISPLAY & DRIVER BD	00405450		24672
V1	LED 7SEG 2CHAR	555600-0352	SP352	73138
V2	LED 7SEG 2CHAR	555600-0352	SP352	73138
V3	LED 7SEG 2CHAR	555600-0352	SP352	73138

REVISIONS					
	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP'D
B	REMOVED CR5 & 6			4-10-72	RJ
C	ADDED R7-R10			6/72	
D	DELETED R1, R3 & R5 RELOCATED R2, R4, R6, R7-R10 DELETE SPACERS (2) ADD ITEM 36 & 37		609	10/72	JHM
E	(4) LED "FLATS" CORRECTED 180°	-	1009	9/12/74	
F	ITEM 37 SHORTENED BY 2 PINS		1098	4/79	SA
G	" " EXTENDED " " "		1109	2/35	
G1	ADDED SH 2 FOR PROD	-	NEC	9/76	
G2	REV. POLARITY CR5, 6		NEC	9/76	
H	DIODES CHANGED, ADDED LED DETAIL ON SHT 2.	-	11621	9/1984	
J	NO. WAS 41766-4-1		4837	1/84	

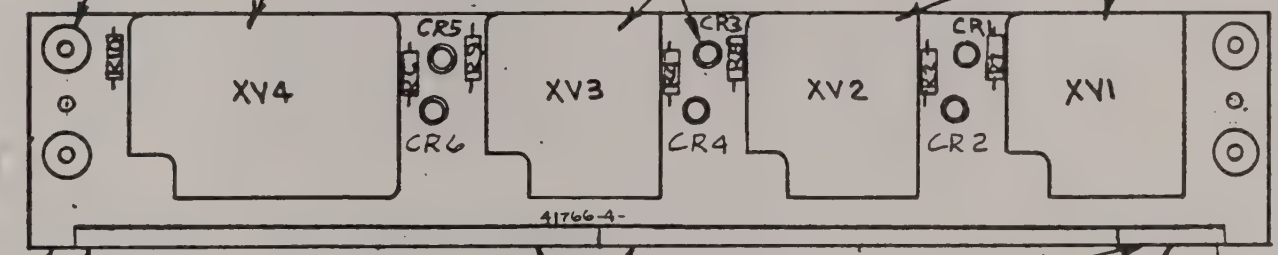
REVISIONS CONTINUED SH 2

LED's MUST BE PERPENDICULAR TO BOARD. INSTALL WITH 520821-0001 SPACER UNDER EACH, 4 PLACES

4-40 x 7/16 SPACER NEAR SIDE
520820-0014
4 PLACES

SOCKET
551005-0006

SOCKET - 3 PLACES
551005-0008



00304766

30 PIN CONNECTOR
551009-0045

SEE NOTE 2

NOTE:

1.) CR 5 & 6 (555600-4480) MOUNTED WITH DAYS OPTION ONLY. (12004945-7)

2.) CUT (551009-0045) TO FIT

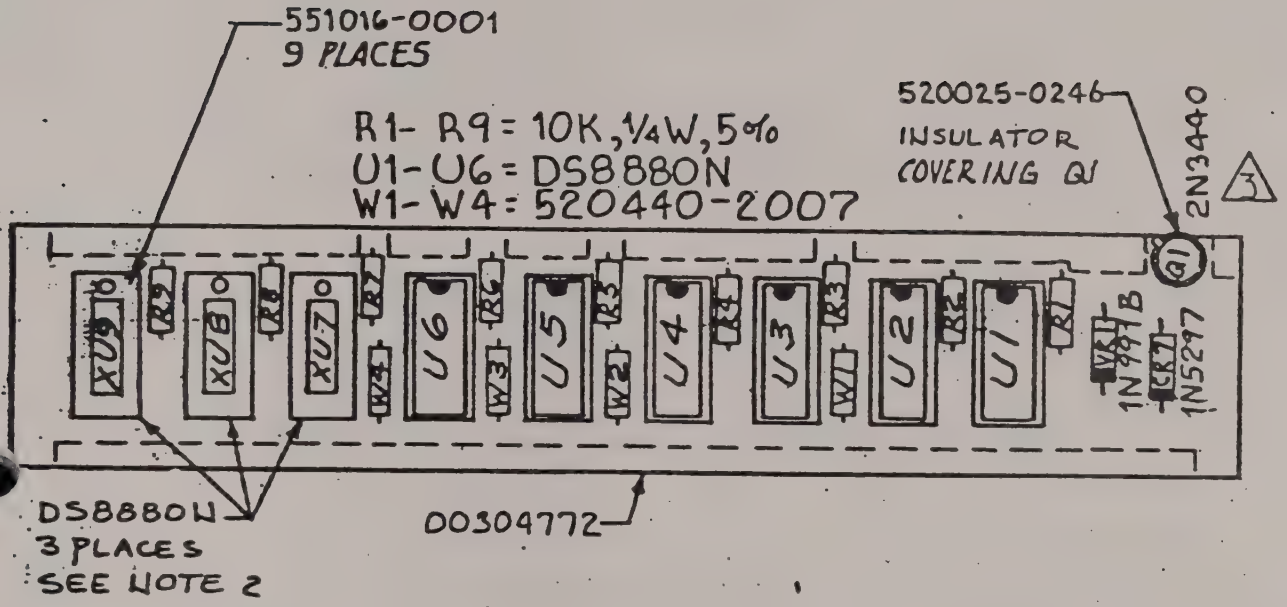
3.) CR1-CR4 ARE P/N. 555600-4480

	DRN 1-20-72	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	AUSTRON AUSTIN, TEXAS	9 DIGIT DISPLAY BOARD
8100A SERIES	CHECK JM DATE ELECT SA DATE MECH SA DATE PROJECT SA DATE APPROVAL N/A DATE		CODE IDENT. 24672	
APPLICATION	SCALE FULL DO NOT SCALE DRAWING	SIZE A SHT 1 OF 2	5-57	DWG NO. 10304766-1 REV L

ASSEMBLY PCB ASSY READOUT,STD 9 DIGIT DIS.
ASSEMBLY NUMBER 10304766-1
REFERENCE DESIGNATOR PREFIX 1A3A102A1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR1MP1	3/16X3/16 SPACER INSUL NYLON	520821-0001	9208-N-115	06540
CR2	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR2MP1	3/16X3/16 SPACER INSUL NYLON	520821-0001	9208-N-115	06540
CR3	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR3MP1	3/16X3/16 SPACER INSUL NYLON	520821-0001	9208-N-115	06540
CR4	.12 LDS 20MA PC LED RED	555600-4480	HLMP-1000	2848
CR4MP1	3/16X3/16 SPACER INSUL NYLON	520821-0001	9208-N-115	06540
MP1	4-40X.437X.25 SPACER ROUND SWG	520820-0014	9536B-A-0440-17	06540
MP2	4-40X.437X.25 SPACER ROUND SWG	520820-0014	9536B-A-0440-17	06540
MP3	4-40X.437X.25 SPACER ROUND SWG	520820-0014	9536B-A-0440-17	06540
MP4	4-40X.437X.25 SPACER ROUND SWG	520820-0014	9536B-A-0440-17	06540
R2	RES FXD COMP 330 OHM 1/4W 10%	651102-0331	RC07GF331K	81349
R4	RES FXD COMP 330 OHM 1/4W 10%	651102-0331	RC07GF331K	81349
R6	RES FXD COMP 330 OHM 1/4W 10%	651102-0331	RC07GF331K	81349
R7	RES FXD COMP 4.7 K 1/4W 10%	651102-0472	RC07GF472K	81349
R8	RES FXD COMP 4.7 K 1/4W 10%	651102-0472	RC07GF472K	81349
R9	RES FXD COMP 4.7 K 1/4W 10%	651102-0472	RC07GF472K	81349
R10	RES FXD COMP 4.7 K 1/4W 10%	651102-0472	RC07GF472K	81349
XA1	CONN 30 PIN RT ANGLE MALE	551009-0045	200264	16512
XA2	CONN 30 PIN RT ANGLE MALE	551009-0045	200264	16512
XV1	SCKT DISPL 2CHAR FOR SP351&2	551005-0008	CS352	73138
XV2	SCKT DISPL 2CHAR FOR SP351&2	551005-0008	CS352	73138
XV3	SCKT DISPL 2CHAR FOR SP351&2	551005-0008	CS352	73138
XV4	SOCKET, DISPL 3 CHAR FOR SP-353	551005-0006	CS-353	73138

BY	DESCRIPTION	REV NO	DATE	APP'D
E	REDRAWN W/NEW A/W (Q1, CR7, VR1).	1440	2/4/82	B.W.
F	NO. WAS 41772-4-1	4837	1/84	
H	ADDED INSULATOR ON Q1	5050	3/84	RJB
J	REVISED PER ECO	7174	3-12-85	OL
K	REVISED PER ECO 7531 BRM		7-25-85	OL
L	REVISED PER ECO 7695 BRM		8-8-85	OL



NOTE

1) DOTTED AREAS TO BE MASKED BEFORE FLOW SOLDERING.

2) FOR USE WITH DAYS OPTION ONLY (12004945-7)

3 INSTALL INSULATOR 520641-0001 UNDER Q1 (2N3440)

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC DES. NO.

DRAWN 3/Feb/81 | CHECK | ELECT. | MECH. | QA | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.1 .XX ±.03 ANGLES ±

AUSTRON INC. AUSTIN, TEXAS

CODE IDENT 20672

9 DIGIT DISPLAY DRIVER BD.

B100 SER ES | NEXT ASSY | APPLICATION | SCALE 1:1 | DO NOT SCALE DRAWING | SH 1 OF 1 | MATERIAL

DRAWING NO. | REF | SIZE | PART NO. | REV
1 | 00304772 | L

5-59

ASSEMBLY PCB ASSY DRIVERS, STD 9 DIGIT DIS.
ASSEMPLY NUMBER 10304772-1
REFERENCE DESIGNATOR PREFIX 1A3A102A2
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	180V .4W 5 DIO ZEN	7011N991B	1N991B	04713
CR7	DIO I REG DO-7 1 MA .6W 100POV	7011N5297	1N5297	81349
Q1	1.0 W TO-39 XSTR NPNS HVAH	7022N3440	2N3440	81349
Q1MP1	INSULATOR TRAN TO 5	520025-0246	#427-327	32559
R1	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R3	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R4	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R5	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R6	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R7	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R8	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R9	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC TTL MSI HIV BCD-7 SEG DEC-DRVR	703DS8880N	DS8880N	27014
U2	IC TTL MSI HIV BCD-7 SEG DEC-DRVR	703DS8880N	DS8880N	27014
U3	IC TTL MSI HIV BCD-7 SEG DEC-DRVR	703DS8880N	DS8880N	27014
U4	IC TTL MSI HIV BCD-7 SEG DEC-DRVR	703DS8880N	DS8880N	27014
U5	IC TTL MSI HIV BCD-7 SEG DEC-DRVR	703DS8880N	DS8880N	27014
U6	IC TTL MSI HIV BCD-7 SEG DEC-DRVR	703DS8880N	DS8880N	27014
W1	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W2	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W3	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W4	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
XU1	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU2	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU3	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU4	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU5	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU6	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU7	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU8	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322
XU9	SOCKET, IC 16 PIN DIP, CLOSED ENT	551016-0001	IC-316-SGT	55322

6. STANDARD OPTIONS

6.1. SCOPE OF SECTION

Section Six provides circuit descriptions, logic and schematic diagrams, assembly drawings, and parts lists for the standard options included with your Model 8120.

6.2. OPTIONS INCLUDED

A number of standard options are available for the Model 8120. Standard options, when supplied with the instrument, will be described on the following pages.

6.2.1. Days/ID (Option E13)
(Block Diagram Dwg. No. 12305008-04)

General Description

The Days/ID Option is shown on the basic instrument block diagram. This option adds the Days Accumulator board (P/N 10302632-21), Leap Year/ID switch S33, a colon and three-digit display to Display Assembly and the associated wiring.

Parallel BCD Days/ID outputs are supplied to connector J3 through buffers on the accumulator board. These twelve-bits have the following specifications:

Code: 8-4-2-1.

Logic: ONE = 5 Vdc $\pm$0.5 Vdc behind 6 kilohm.

ZERO = 0 $\pm$0.5 Vdc, 12 mA sink.

All outputs are short-circuit-proof to ground.

An ID Update input (IC levels) to rear panel BNC connector J13 is provided. This input is fed to a circuit on the Modulator (A20).

6.2.2. Days Accumulator
(Schematic Dwg. No. 12302632-21)

The Days Accumulator board can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit is included which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days.

Decade Divider Circuits

The up-to-date decade dividers are connected in tandem. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe (PRESET) line is grounded. The decade zero-reset inputs are wired in common through buffers on (U8) to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

Output Buffer Circuits

The BCD output buffers may be inverting or non-inverting. One of the two sets (U10), (U13) and (U15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters (U11).

Input Inhibit Circuit

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate (U2,6) inverts and buffers the input. Gates (U2,11) and (U2,8) form an RS flip-flop.

(U2,3) gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop (U2,8 and 11) output follows the input. When the INHIBIT line, pin H, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the INHIBIT line.

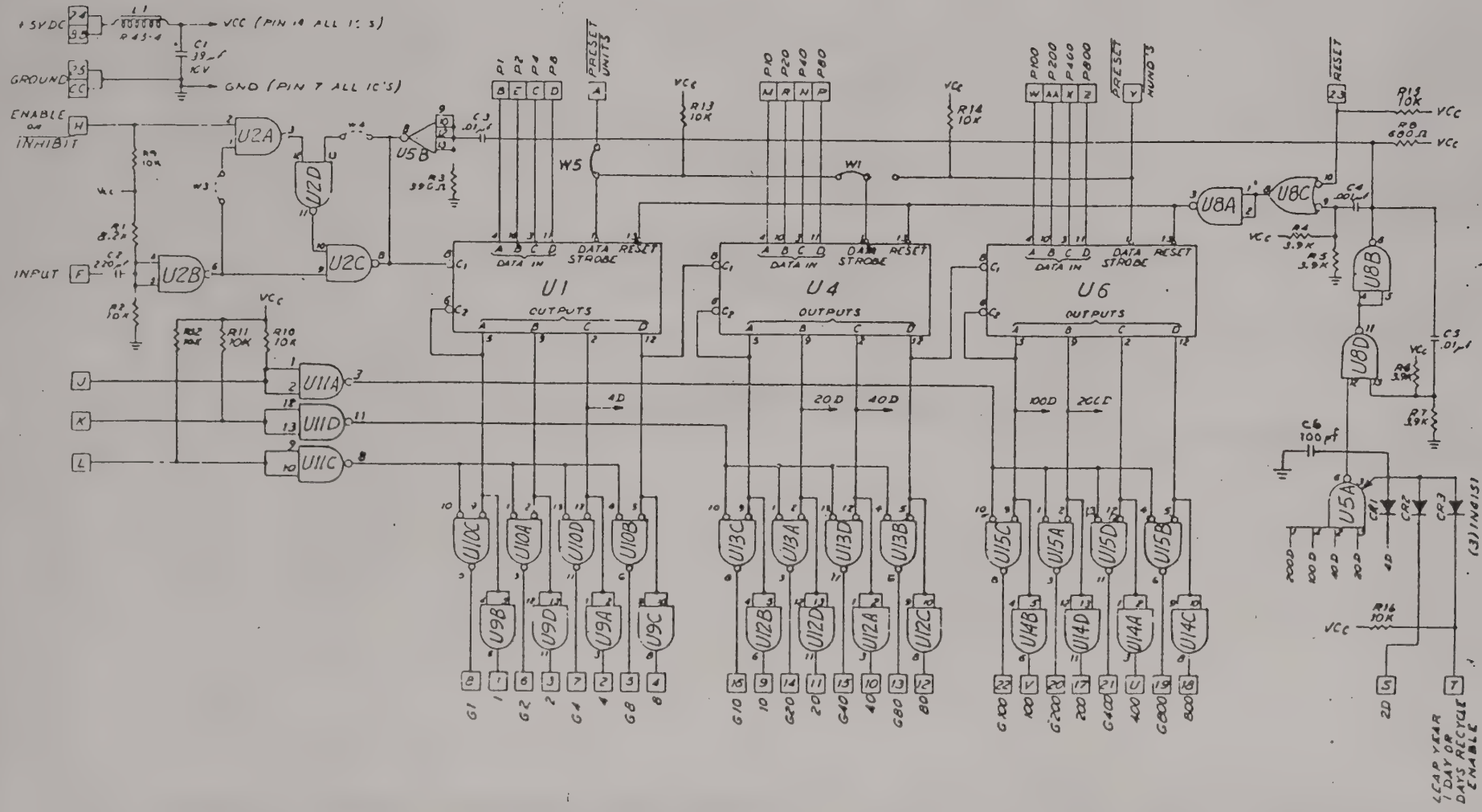
Days Recycle Circuit

Gate (U5,6) is a four-input NAND gate with an expander input. The connection of diodes CR1 through CR3 gives the gate seven inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for leap year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the two-day output. At the selected count, the output of (U5,6) will go low, triggering one-shot (U8,11 and 6). The one-shot output is a negative-going pulse (from 5 Vdc to 0 Vdc). The leading edge of the pulse (ac-coupled into U8,8) causes the three dividers to reset to 000. The trailing edge of the pulse (which is positive-going) is ac-coupled into (U5,8) where it is inverted and used to input one count to the first decade. The resulting accumulator contents are 001.

2

3

REVISIONS					
ZONE	LTR	DESCRIPTION	ECO	DATE	APPD
	B	ADDED C6	11556	6/78	P
	C	DWG NO. WAS 21632-7-21	4837		
	D	CHGD. IC REF DES FROM A TO U	6557	9-19-84	OK
	E	REVISED PER ECO 7355	—	4-29-85	OK



3. FOR TENS TO PRESET WITH UNITS, INSTALL W1 AND NOT W2.
2. C3 USED FOR DAYS RECYCLE TO 1.
1. IC TYPES AS FOLLOWS:

U1,4 & 6 = 74176
U2 & 11 = MC846P
U5 = MC830P
U8 = SN7400N
U9,12 & 14 = MC1006P
U10,13 & 15 = MC1008P

NOTES:

NEXT ASSY	USED ON	REF DES	FIG NO.
	8155		

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED

DEC	FRAC	ANG

MATERIAL:

ENGR	[illegible] M	10-74
CHECK		
DRAWN	R	10-74

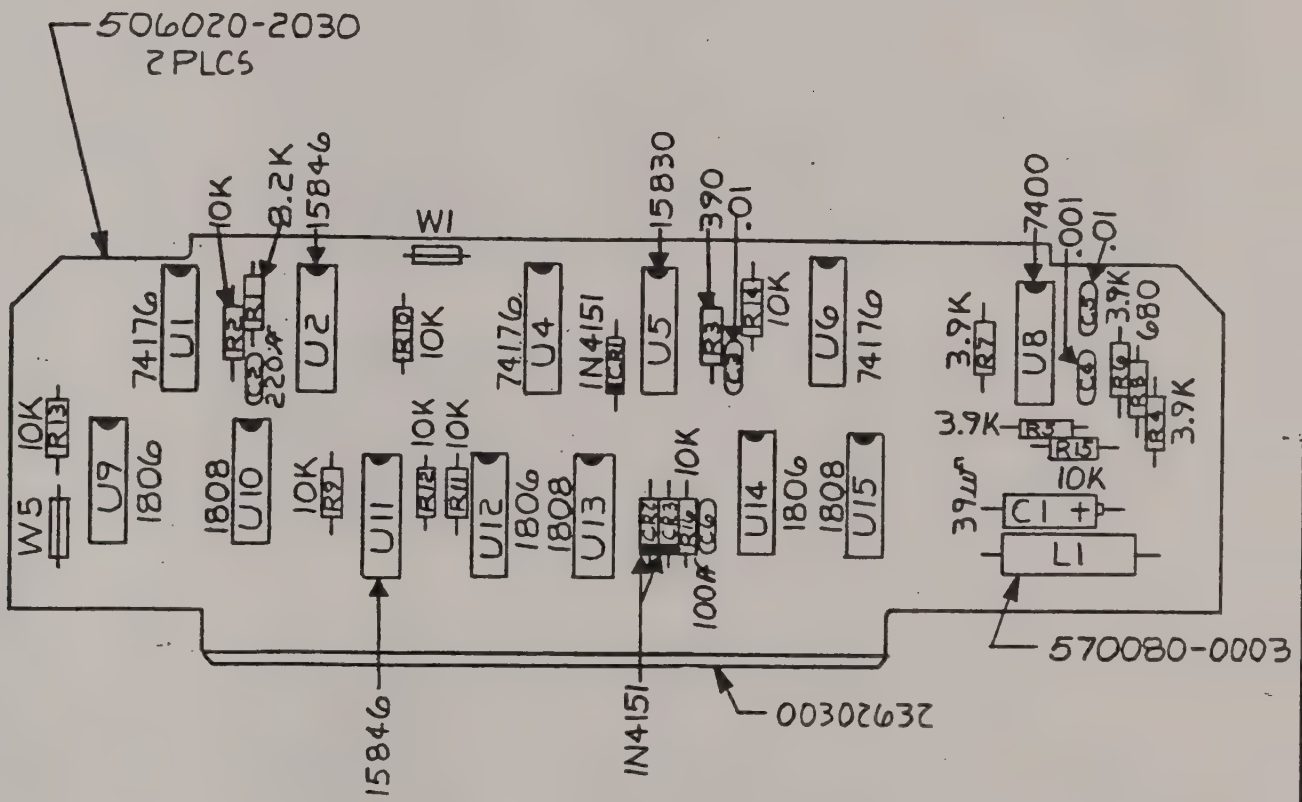
AUSTRON INC.
AUSTIN, TEXAS

SCHEMATIC, DAYS ACCUMULATOR

SIZE	CODE IDENT NO.		REV
2	24672	12302632-21	E

SCALE | SHEET OF

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
D	RELEASED	11-7-84	OR
E	REMOVED "W4" PER ECO 8085	3/27/85	OR
F	REVISED PER ECO 7355	4-29-85	OR
G	REVISED PER ECO 7534	7-1-85	OR



		TOLERANCES UNLESS OTHERWISE SPECIFIED			AUSTRON INC. AUSTIN, TEXAS	
		DEC	FRAC	ANG	ACCUMULATOR, 3 DIGIT BUFFERED	
		MATERIAL:				
	8100	ENGR		11-7-84	SIZE 1	CODE IDENT NO. 24672	10302632-21	REV G
NEXT ASSY	USED ON	CHECK		11-7-84				
APPLICATION		DRAWN		11-6-84	SCALE 1/1		SHEET 1 OF 1	

ASSEMBLY PCB ASSY 3 DIGIT ACCUMULATOR W/BUF
ASSEMBLY NUMBER 10302632-21
REFERENCE DESIGNATOR PREFIX 1A3A21
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
CR1	50V DIO SIG	7011N4151	1N4151	13715
CR2	50V DIO SIG	7011N4151	1N4151	13715
CR3	50V DIO SIG	7011N4151	1N4151	13715
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	220 PF 1KV DISC CERAMIC	601014-0221	DD-221	71590
C3	.01 UF 100V 20 CAP CERAMIC	601004-0103	TG-S10	56289
C4	.001 UF 1KV 20CAP	601011-0102	5GAD10	56289
C5	.01 UF 100V 20 CAP CERAMIC	601004-0103	TG-S10	56289
C6	100 PF 500V 5 CAP DIP MICA	603000-0101	DM15-101J	02799
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 8.2 K 1/4W 10%	651102-0822	RC07GF822K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R3	RES FXD COMP 390 OHM 1/4W 10%	651102-0391	RC07GF391K	81349
R4	RES FXD COMP 3.9 K 1/4W 10%	651102-0392	RC07GF392K	81349
R5	RES FXD COMP 3.9 K 1/4W 10%	651102-0392	RC07GF392K	81349
R6	RES FXD COMP 3.9 K 1/4W 10%	651102-0392	RC07GF392K	81349
R7	RES FXD COMP 3.9 K 1/4W 10%	651102-0392	RC07GF392K	81349
R8	RES FXD COMP 680 OHM 1/4W 10%	651102-0681	RC07GF681K	81349
R9	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R10	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R11	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R12	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R13	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R14	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R15	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R16	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC PST DEC CNTR/LATCH	703SN74196N	SN74196N	01295
U2	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U4	IC PST DEC CNTR/LATCH	703SN74196N	SN74196N	01295
U5	IC DUAL 4-IN NAND GATES	703SN15830N	SN15830N	01295
U6	IC PST DEC CNTR/LATCH	703SN74196N	SN74196N	01295

ASSEMBLY PCB ASSY 3 DIGIT ACCUMULATOR W/BUF (CONT)
ASSEMBLY NUMBER 10302632-21
REFERENCE DESIGNATOR PREFIX 1A3A21
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
U8	IC QUADR 2-INP NAND GATE	703SN7400N	SN7400N	01295
U9	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U10	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713
U11	IC QUAD 2-IN NAND GATES	703SN15846N	SN15846N	01295
U12	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U13	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713
U14	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U15	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713

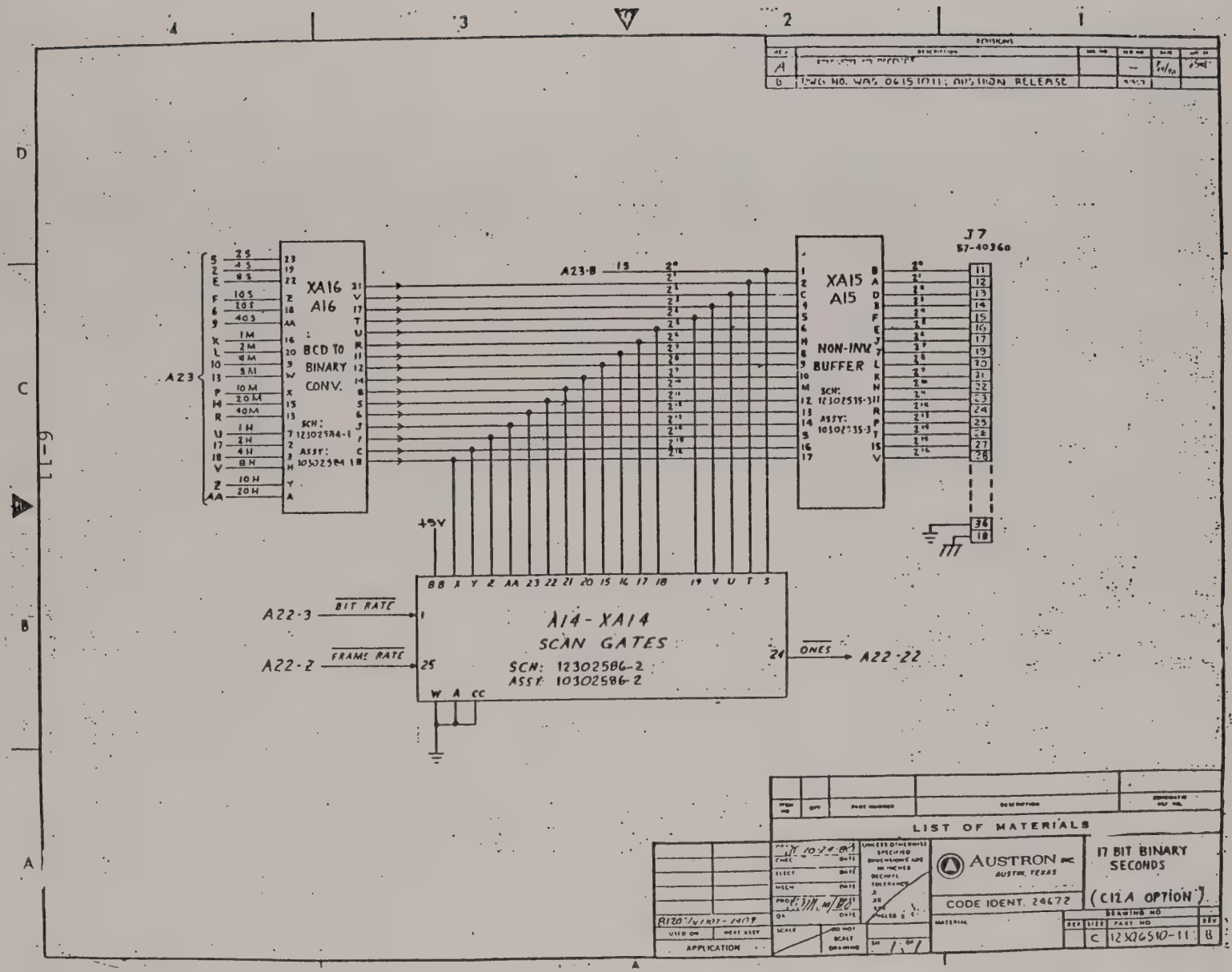
ASSEMBLY P/L OPT E14,MILLISEC
ASSEMBLY NUMBER 12805926-1
REFERENCE DESIGNATOR PREFIX 1
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A2J6	CONN 14 PIN SOCKET CHASSIS RCPT	551306-0005	57-40140	02660
	** SHIP WITH **			
P6	CONN 14 PIN PLUG	551306-0000	57-30140	02660

6.2.3. 17-Bit Binary Seconds (Option C12A) (Schematic Dwg. No. 12306510-11)

General Description

This option converts BCD Time-of-Day in hours, minutes and seconds to 17-bits binary seconds in serial form for insertion in the IRIG B Time Code. BCD to Binary Converter, A16, accepts parallel BCD TOD from TOD Accumulator, A23, and converts it to parallel binary seconds which are serialized by Scan Gates on A14. The serial output from A14 is fed to Code Generator, A22, for insertion in the Time Code. Parallel Binary TOD is fed through buffers on A15 to rear panel connector, J7.


REVISIONS
A
B
DWG NO. WAS 06151011; ADDITION RELEASE
XA16
A16
BCD TO
BINARY
CONV.
SCH: 12302584-1
ASSY: 10302584-1
A23
A23-B
XA15
A15
NON-INV
BUFFER
SCH: 12302535-3
ASSY: 10302535-3
J7
57-40360
+5V
A14 - XA14
SCAN GATES
SCH: 12302586-2
ASSY: 10302586-2
A22-3
BIT RATE
A22-2
FRAME RATE
ONES
A22-22
LIST OF MATERIALS
AUSTRON INC
AUSTIN, TEXAS
CODE IDENT. 24672
17 BIT BINARY
SECONDS
(C12A OPTION)
DRAWING NO
12302510-11
APPLICATION

ASSEMBLY OPTION (C12A) 17 BIT BINARY SEC.
ASSEMBLY NUMBER 12806510-11
REFERENCE DESIGNATOR PREFIX 1A3
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A14	PCB ASSY SCAN GATES	10302586-2		24672
A15	PCB ASSY, 20 BIT BUFFER	10302535-3		24672
A16	PCB ASSY BCD TOD- 17 BIT BINARY	10302584-1		24672
A2J7	CONN 36 SOCKET CHASSIS RECEPTACLE	551306-0030	57-40360	02660
XA14	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA15	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
XA16	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DREI	54453
	* SHIP WITH *			
P7	CONN, 36 PIN PLUG	551306-0035	57-30360	02660

6.2.4. IRIG A, B, & E17 Bit Scan Gates (Schematic Dwg. No. 12302586-02)

General Description

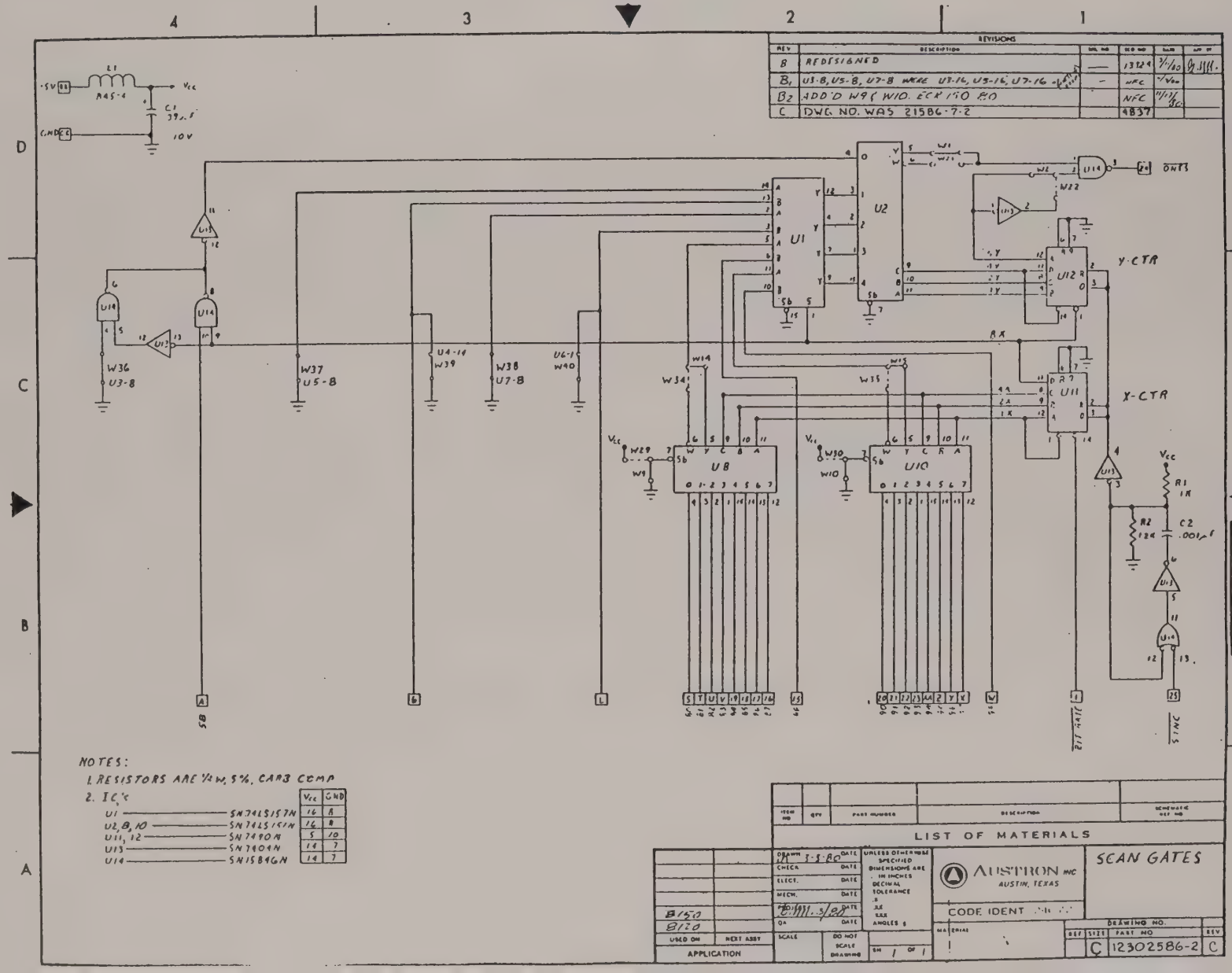
The purpose of this assembly is to accept seventeen bits of information in parallel and to serialize them into a level shift code. The format is fixed so that the assembly can be used as an extension for the IRIG Code Generator Assembly, Dwg. No. 10302554-01. The seventeen bits are inserted at the end of the time code frame. The parallel inputs are supplied from the TOD Accumulator.

Circuit Description

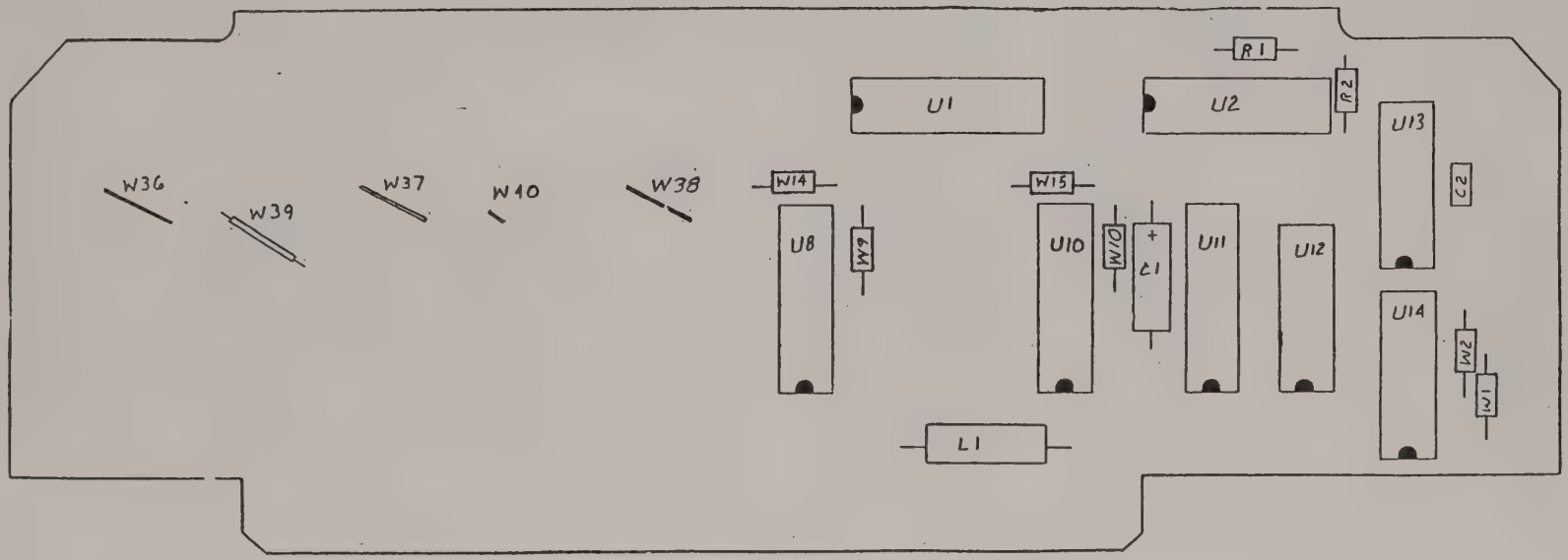
Scanning is accomplished through the two-stage switching action of (U1), (U8) and (U10) (first stage) and (U2) (second stage). These electronic switches are controlled by decade counters (U11) and (U12) which are driven at the time code bit rate. In the case of IRIG B, for example, the bit rate is 100 pps. Both decades are synchronized to the time code frame by the SYNC input to pin 25. This signal resets the counters at the start of each frame.

Decade (U11) controls first stage switching. It is connected in the conventional 1, 2, 4, 8 configuration. The first three bits control eight-bit data selectors (U8) and (U10). The fourth bit controls quad two-bit data selector (U1). These selectors sequentially place three groups of zeros (nine bits each) followed by each of the nine bits in the two active input groups onto the five input lines to eight-bit data selector (U2).

Decade (U12) controls second stage switching, data selector (U2). It is connected in the unconventional 1, 2, 4, 5 configuration. The first three bits control (U2) which feeds each of five, 9-bit data streams from the first stage to NAND gate (U14,3) twice each time code frame, once during the first half and again during the second half of the frame. The fourth bit from (U12,5 and Y) controls gate (U14,3) feeding the data (ONES) via pin 24 to the Code Generator only during the second half of the frame (Jumper W2 installed). Thus, the forty-five bits (seventeen active) are inserted into the frame at locations 50 through 58, 60 through 68, 70 through 78, 80 through 88 and 90 through 98. The Code Generator automatically inserts markers in locations 59, 69, 79, 89 and 99, overriding the ONES signal. The seventeen active bits are in 80 through 88 and 90 through 97.


REVISIONS
REV
DESCRIPTION
B
REDESIGNED
B1
U3-8, U5-8, U7-8 WERE U3-14, U5-14, U7-14
B2
ADD'D W9 (W10. ECR 1510 R0
C
DWG. NO. WAS 21586-7-2
NOTES:
1. RESISTORS ARE ¼W, 5%, CARB COMP
2. IC's
U1 — SN74LS157N
U2,8,10 — SN74LS(S)74N
U11,12 — SN7490N
U13 — SN7404N
U14 — SN7584GN
LIST OF MATERIALS
SCAN GATES
AUSTRON INC
AUSTIN, TEXAS
CODE IDENT
DRAWING NO.
12302586-2
APPLICATION
B1S0
B120

REV	DESCRIPTION	ECN NO	DRN	DATE	APP'D
A	REDESIGNED	—	13924	1/80	
A1	REMOVED W29 & 30; ADD'D W9 & W10	ECN 150 80	NFC	1/80	
B	DWG WAS 021586-4-Z ECO 4837				



LIST OF MATERIALS

AUSTRON INC AUSTIN, TEXAS

PC Assy

CODE IDENT 52542

B 1002586-2

APPLICATION

A150
A120

6-15

ASSEMBLY PCB ASSY SCAN GATES
ASSEMBLY NUMBER 10302586-2
REFERENCE DESIGNATOR PREFIX 1A3AX
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
C2	CAP CERA RDL COG 1000 PF 100V 5%	601110-0102	CN20A102J242	71590
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 1 K 1/4W 10%	651102-0102	RC07GF102K	81349
R2	RES FXD COMP 1.2 K 1/4W 10%	651102-0122	RC07GF122K	81349
U1	IC QUAD 2-1 DATA SELECTORS/MULTIPLE	703SN74LS157	SN74LS157N	01295
U2	IC 1-OF-8 DATA SELECTOR/MULTIPLEXER	703SN74LS151	SN74LS151N	01295
U8	IC 1-OF-8 DATA SELECTOR/MULTIPLEXER	703SN74LS151	SN74LS151N	01295
U10	IC 1-OF-8 DATA SELECTOR/MULTIPLEXER	703SN74LS151	SN74LS151N	01295
U11	IC DECADE COUNTER	703SN74LS90N	SN74LS90N	01295
U12	IC DECADE COUNTER	703SN74LS90N	SN74LS90N	01295
U13	IC HEX INVERTER	703SN74LS04N	SN74LS04N	01295
U14	IC MDTL QUAD 2 INPUT NAND GATE	703MC846P	MC846P	04713
W1	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W2	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W9	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W10	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W14	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W15	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W26	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W37	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W38	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210
W40	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210

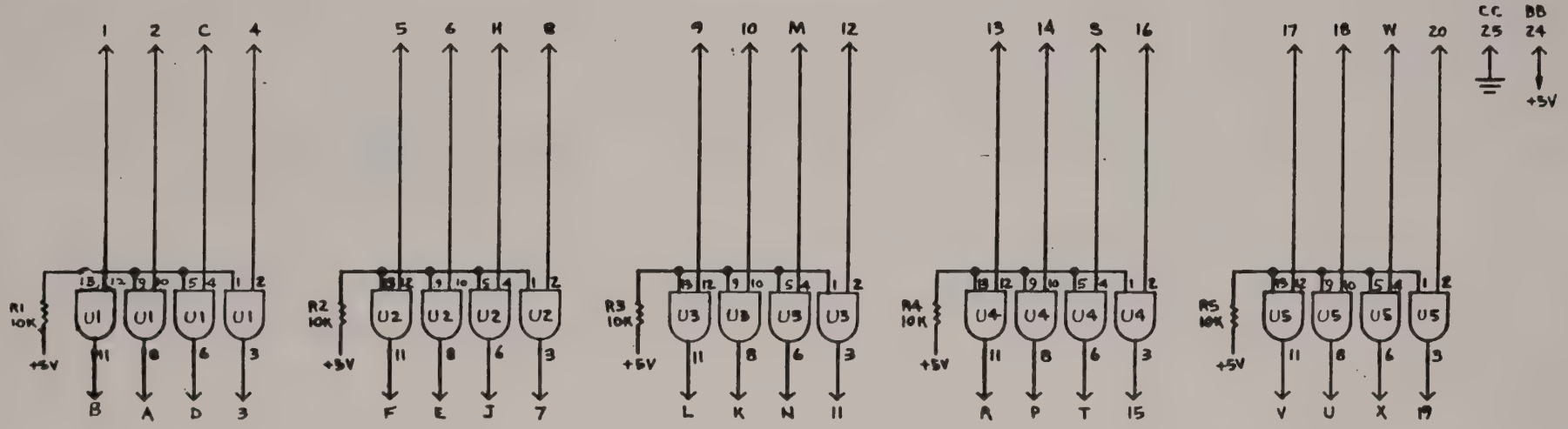
6.2.5. Buffer Assembly
(Schematic Dwg. No. 12302535-03)

The Buffer Assembly PCB contains twenty integrated-circuit gates, connected as non-inverting buffers. The circuit buffers the seconds-through hours output of the Time of Day Accumulators.

ONE = 5 Vdc ($\pm$0.5 Vdc) 6 kilohm source.

ZERO = 0 Vdc ($\pm$0.5 Vdc), 12 mA sink.

-1	UPDATED TITLE BLOCK	–	6-7	VM
A	TRANSFERRED FROM 9 dwg, ADD DRAWING OF A1 THRU A5 AN SCH A	–	9-30	VM
A1	SCH. RMS FOR 21535-7-16 ALSO.	–	NR	VM
B	DWG No. WAS 21535-7-3		4017	



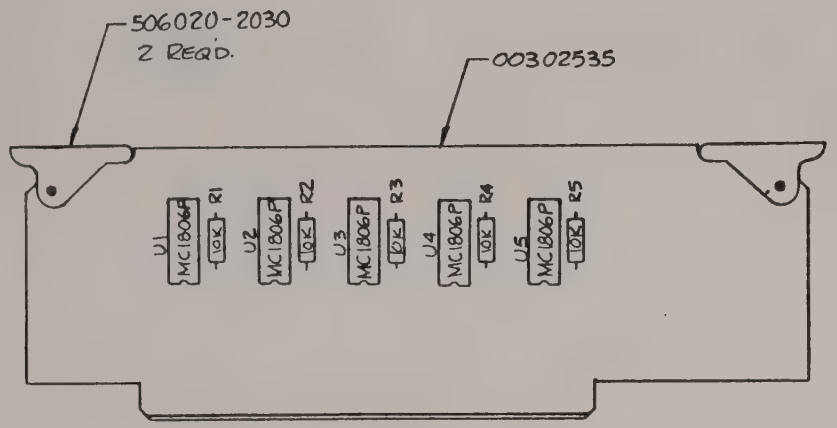
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & PIN 7 " " " " " " GRD.
3. U1 THRU U5 ARE MC1506P

5190		AUSTRON AUSTIN, TEXAS	SCHEMATIC 20 BIT BUFFER NON-INVERTING	
1121			125025353	8

6-18

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPD
	A	DWG NO. WAS 21535-4-3 EC04837		
	B	REVISED PER ECO 6557	10JUN	



6-19

NEXT ASSY	USED ON	REF DES	FIG NO.
	8130		
	8121		
APPLICATION			

TOLERANCES UNLESS OTHERWISE SPECIFIED: DEC | FRAC | ANG

MATERIAL:

ENGR	G.M.	9-68
CHECK	S-D	9-68
DRAWN	RBW	9-68

AUSTRON INC. AUSTIN, TEXAS

PC B ASSY, 20 BIT BUFFER

SIZE	CODE IDENT NO.		REV
2	24672	10302535-3	B
SCALE 1:1		SHEET 1 OF 1	

ASSEMBLY PCB ASSY, 20 BIT BUFFER
ASSEMBLY NUMBER 10302535-3
REFERENCE DESIGNATOR PREFIX 1A3AX
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
R1	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R2	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R3	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R4	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
R5	RES FXD COMP 10 K 1/4W 10%	651102-0103	RC07GF103K	81349
U1	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U2	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U3	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U4	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713
U5	IC QUAD 2-IN AND GATES	703MC1806P	MC1806P	04713

6.2.6. BCD Time-of-Day to 17-Bit Binary Converter (Schematic Dwg. No. 12302584-01)

General Description

This circuit PCB performs a parallel conversion of a grouped BCD number representing the time-of-day in seconds, minutes, and hours to a single seventeen-bit binary number representing the time-of-day in seconds.

The conversion is performed in two steps. First, each BCD group is converted to a binary group so that there is a six-bit binary number representing seconds of the minute, a six-bit binary number representing minutes of the hours, and a five-bit number representing the hour of the day. The second step is to weight the minutes and hours bits in terms of seconds and add them to the second bits to produce a straight binary number. Where the desired result is the group binary number, the second step is omitted. Provision is made on the PCB to omit the adders for the second conversion and to jumper the group binary outputs to the output pins shown at the bottom of the schematic. Positive logic is employed, throughout, where 5 V represents a logical ONE and ground a logical ZERO.

Circuit Description

Conversion from Group BCD to Group Binary. This circuitry is shown on the top half of the schematic and consists of three independent circuits. Two of them, the seconds and minutes, are identical.

The operation is best understood when a chart is drawn showing the BCD bit weights vertically and the desired binary weights across the top. Now by breaking each BCD bit into its binary equivalent (bits 10 and higher) and assigning these to the proper column, the columns can be summed, allowing carries (as depicted, to the right) and arrive at the binary equivalent to the BCD number.

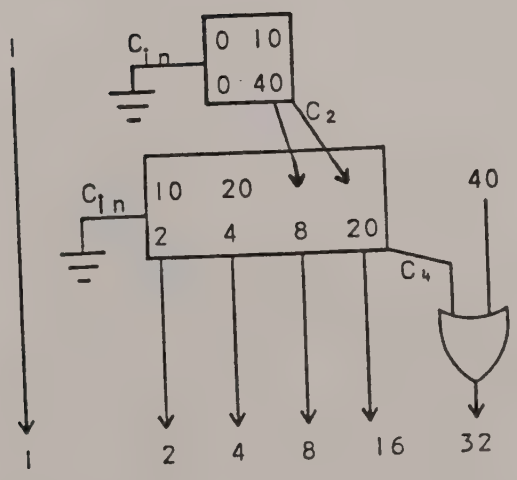
		2^0	2^1	2^2	2^3	2^4	2^5	← BINARY POSITION
		1	2	4	8	16	32	← WEIGHTS
	1	1						
	2		2					
BCD	4			4				
WEIGHTS	8				8			
	10		10		10			
	20			20		20		
	40				40		40	
RESULTANT ADDITION TO BE PERFORMED		1	2	4	8	20	40	
			10	20	10			
					40			
		Σ_0	Σ_1	Σ_2	Σ_3	Σ_4	Σ_5	

BCD SECONDS OR MINUTES CONVERSION TO BINARY

BCD Seconds/Minutes Conversion to Binary.

NOTE

The addition is performed by the use of dual and quad full adders and is shown schematically below.



Schematic, Use of Dual & Quad Full Adders.

Note that the units-of-seconds is not changed in the conversion and hence does not appear on the final circuit board. The actual circuitry for seconds conversion is (U10), (U11), (U12) and part of OR gate (U13). IC (U11) is used strictly for buffering to reduce loading on the inputs. The "minutes" circuitry consists of (U14), (U15), (U16), another (U13) OR gate, and two (U8) gates for buffering units-of-minutes. The "hours" conversion is somewhat simpler since the full scale is 23 instead of 59 and hence no BCD "40". There is no need for the separate adder or the OR gate. The conversion is done by (U18) with buffering of the inputs done by parts of gates (U3), (U17) and (U13).

Conversion from Group Binary to Straight Binary. This circuitry is shown on the bottom half of the schematic and consists of quad adders, inverters and quad adders used as subtracters. Again, the operation is best seen by drawing the weighting chart.

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16,384	32,768	65,536
1S	1S															
2S		2S														
4S			4S													
8S				8S												
16S					16S											
32S						32S										
1M			1M	1M	1M	1M										
2M				2M	2M	2M	2M									
4M					4M	4M	4M	4M								
8M						8M	8M	8M	8M							
16M							16M	16M	16M	16M						
32M								32M	32M	32M	32M					
1H					1H					1H	1H	1H				
2H						2H					2H	2H	2H			
4H							4H					4H	4H	4H		
8H								8H					8H	8H	8H	
16H									16H					16H	16H	16H

Weighting Chart.

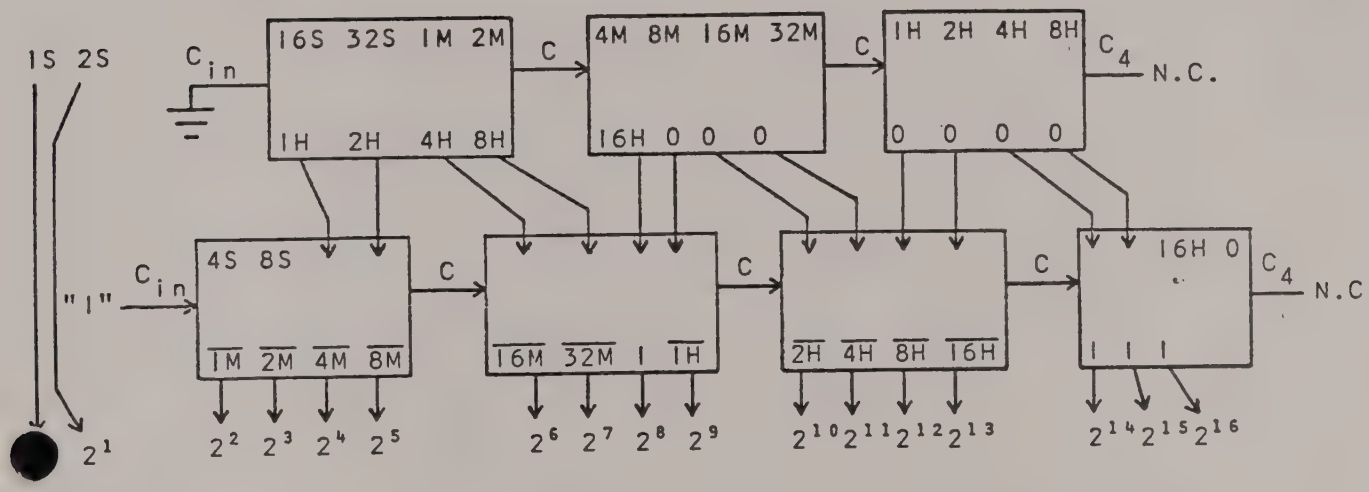
This approach represents a log of additions. However, it can be simplified considerable if we utilize subtraction as well as addition. For example, one minute can be represented by 64-4 instead of 32+16+8+4. Applying this philosophy to all the minutes and hours terms and representing a negative number by a bar over its symbol, we arrive at the following chart.

	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16,384	32,768	65,636
1S	1S																
2S		2S															
4S			4S														
8S				8S													
16S					16S												
32S						32S											
1M			$\overline{1M}$				1M										
2M				$\overline{2M}$				2M									
4M					$\overline{4M}$				4M								
8M						$\overline{8M}$				8M							
16M							$\overline{16M}$				16M						
32M								$\overline{32M}$				32M					
1H					1H					$\overline{1H}$			1H				
2H						2H					$\overline{2H}$			2H			
4H							4H					$\overline{4H}$			4H		
8H								8H					$\overline{8H}$			8H	
16H									16H					$\overline{16H}$			16H

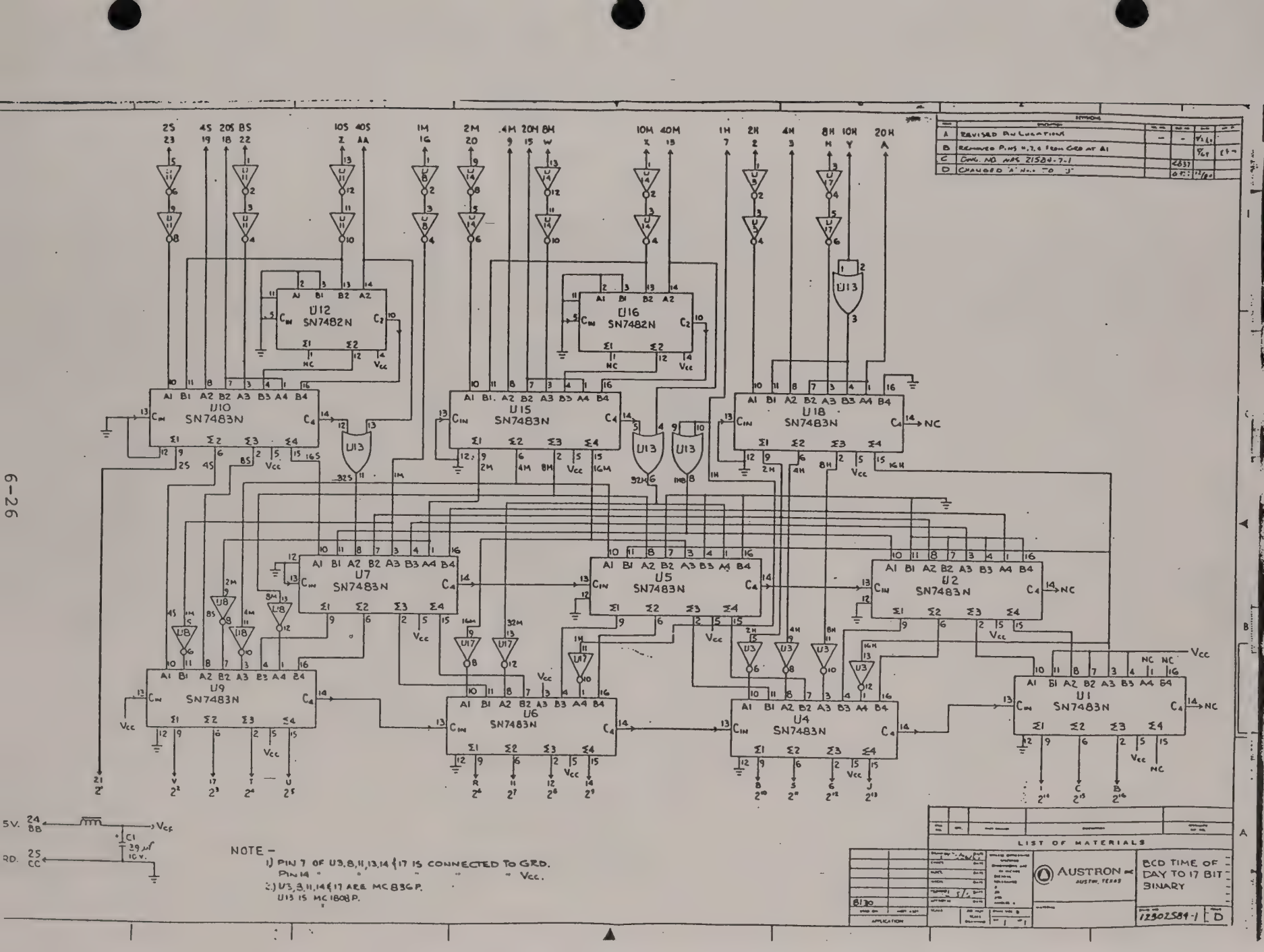
Addition and Subtraction Chart.

Using quad adders, the summation of the group binary bits is performed as follows

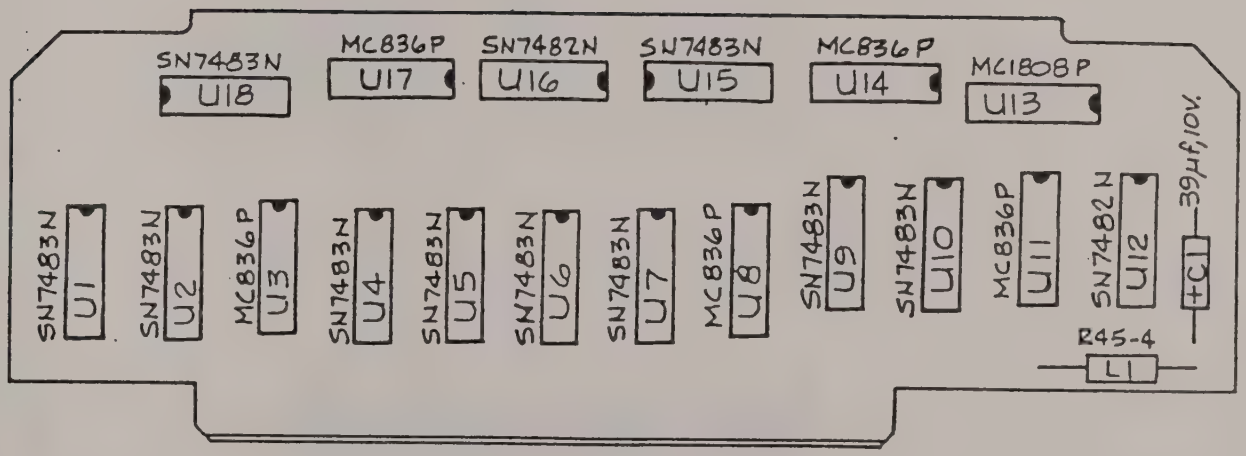
Summation of Group Binary Bits Chart.



The subtraction is performed by adding the one complement of the negative number and supplying the end-around carry as a hard-wired ONE (Vcc) to the carry in, C (IN), terminal of (U9). The end-around carry must always be a ONE because the final binary number is always positive (or zero). The ONEs complements are created by the inverters (U8), (U17) and (U3).


2S 4S 20S 8S
10S 40S
1M 2M 4M 20M 8M
10M 40M
1H 2H 4H 8H 10H 20H
U12 SN7482N
U16 SN7482N
U13
U10 SN7483N
U15 SN7483N
U18 SN7483N
U7 SN7483N
U5 SN7483N
U2 SN7483N
U9 SN7483N
U6 SN7483N
U4 SN7483N
U1 SN7483N
U8
U17
U3
Vcc
NC
NOTE –
1) PIN 7 OF U3,8,11,13,14 & 17 IS CONNECTED TO GRD.
PIN 14 " " " " Vcc.
2) U3,8,11,14 & 17 ARE MC836P.
U13 IS MC1808P.
5V. 24 BB
RD. 25 CC
C1 39 µf 10 V.
LIST OF MATERIALS
AUSTRON INC AUSTIN, TEXAS
BCD TIME OF DAY TO 17 BIT BINARY
12302589-1 D
6-26

REVISIONS					
LTR	DESCRIPTION	ECN NO	DRAWN	CHK'D	APP'D
A	DWG WAS 21584-4-1		4-28-71		



DRAWN		4/28/71	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.03 .XX ±.01 ANGLES ±	AUSTRON INC AUSTIN, TEXAS	ASSEMBLY P.C. BOARD BCD T.O.D. TO 17 BIT BINARY
CHECK					
ENGR					
MFGR		4/30/71			
APPROVAL					
8130		SCALE 1-1	DWG SIZE A	MATERIAL	DWG NO. 10302584-1 A
APPLICATION					

ASSEMBLY PCB ASSY BCD TOD- 17 BIT BINARY
ASSEMBLY NUMBER 10302584-1
REFERENCE DESIGNATOR PREFIX 1A3AX
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C1	39 UF 10V 10 CAP TANT	608114-0396	150D396X9010B2	56289
L1	BEAD, FERRITE	570080-0003	R-45-4	42498
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
U1	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U2	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U3	IC HEX INV 6K PULL-UPS	703MC836P	MC836P	04713
U4	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U5	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U6	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U7	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U8	IC HEX INV 6K PULL-UPS	703MC836P	MC836P	04713
U9	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U10	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U11	IC HEX INV 6K PULL-UPS	703MC836P	MC836P	04713
U12	IC 2-BIT BIN FULL ADDER	703SN7482N	SN7482N	01295
U13	IC QUAD 2-IN OR GATES	703MC1808P	MC1808P	04713
U14	IC HEX INV 6K PULL-UPS	703MC836P	MC836P	04713
U15	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295
U16	IC 2-BIT BIN FULL ADDER	703SN7482N	SN7482N	01295
U17	IC HEX INV 6K PULL-UPS	703MC836P	MC836P	04713
U18	IC 4-BIT BIN FULL ADDER	703SN7483N	SN7483N	01295

6.2.7. DC Code Output
(Schematic Dwg. No. 12307743-04)

General Description

This special feature adds a buffered DC Code output to the basic unit equipped with Serial Binary TOD Option C12A.

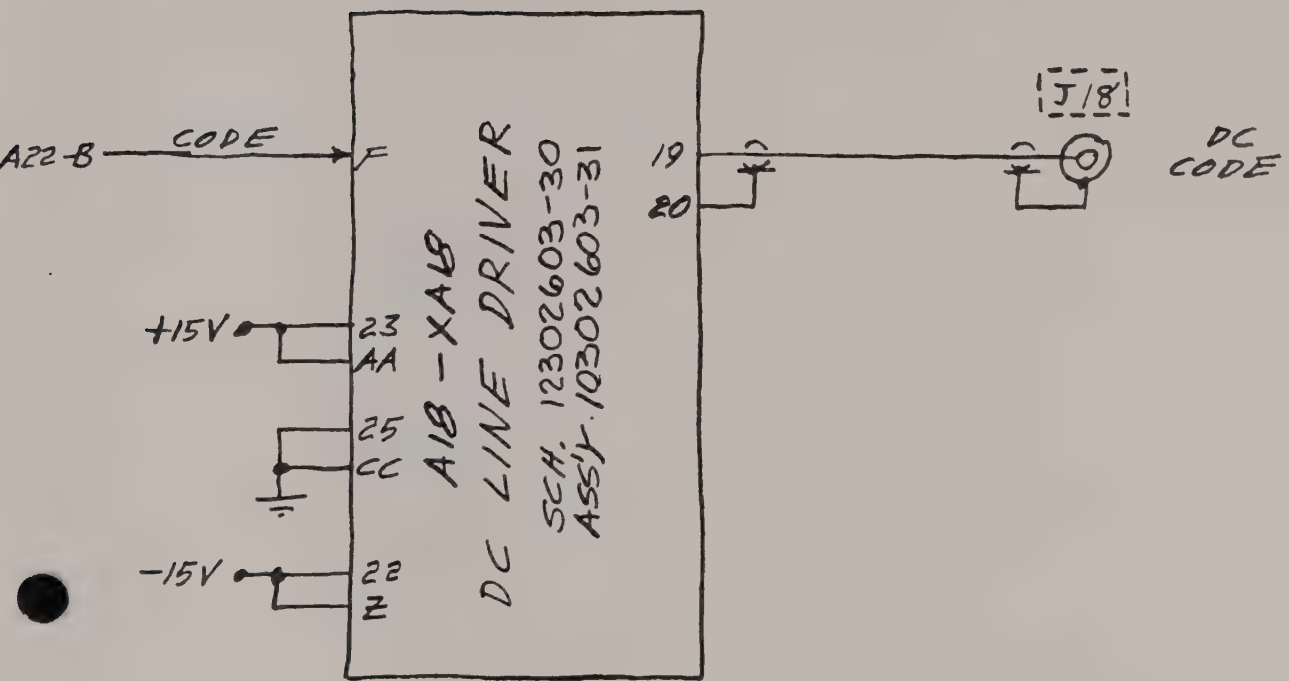
Specifications

This output is driven by an SN54S140J 50 ohm line driver. The DC Code output is positive level, positive true in the IRIG B format complete with 17-bit binary seconds.

Circuit Description

The output from the line driver is wired to rear panel BNC J18.

REVISIONS					
ZONE	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP. BY
A	RELEASED TO RECORDS			9/4/81	RH
B	NO. WAS 07174304		4831	2/84	



NOTES:

1. THE CIRCUIT SHOWN IS SUPERIMPOSED ON THE BASIC UNIT (REFERENCE BLOCK DIAGRAM 12405.008-4).
2. BNC J18 IS MOUNTED ON THE REAR PANEL.

		DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.01 .XXX ±.005 ANGLES ±	AUSTRON INC AUSTIN, TEXAS	BUFFERED DC CODE OUTPUT (50 Ω)
		CHECK	DATE			
		ELECT	DATE			
		MECH	DATE		CODE IDENT. 24672	
B120	4N1407	Q.A.	DATE		MATERIAL	REF 7
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING	DWG SIZE A	DWG NO 1230T1434	ISSUE B
APPLICATION				SH 1 OF 1		

ASSEMBLY OPT. BUFFERED DC CODE OUT
ASSEMBLY NUMBER 12807743-4
REFERENCE DESIGNATOR PREFIX 1
QUANTITY EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
A18	PCB ASSY DC LINE DRIVER	10302603-31		
A2J18	CONN, BNC	551100-1094	UG-1094A/U	74868
MP1	INSULATOR UG 1094/U BNC	520025-1094	10221N	07047
MP2	WASH FIBER FLAT .380.X630X.016	510900-0016	F-7716-380	61000
MP3	3/8X7/8X.017 SOLDER LUG BR	520505-0375	1497	83330
XA18	CONN 25 POS DUAL READOUT SOLTAB W/T	551009-0040	RZM25DRET	54453

6.2.8. DC Line Driver
(Schematic Dwg. No. 12302603-30)

General Description

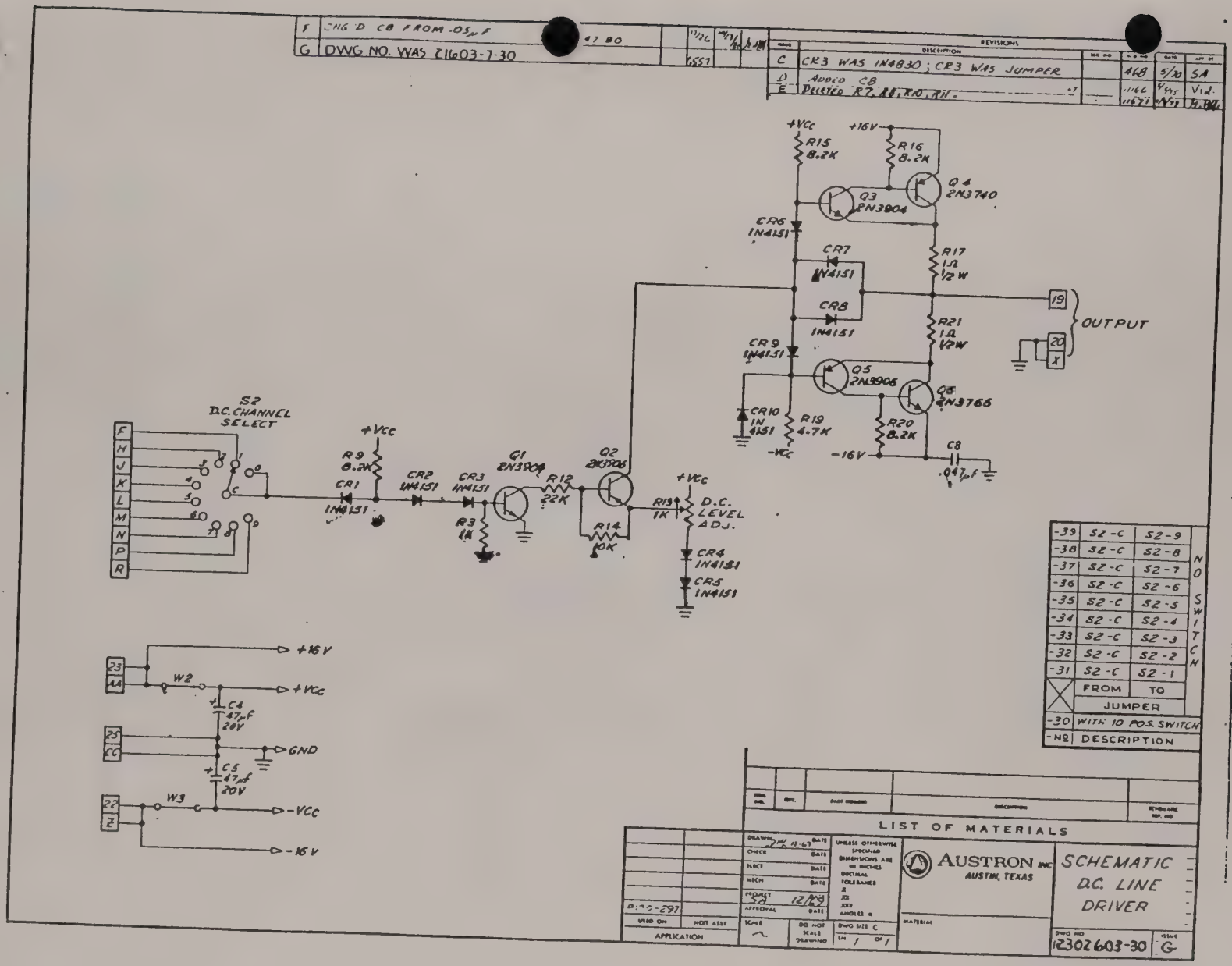
The Line Driver is used when the requirement exists to drive low impedance dc loads. The input looks like a DTL gate whose output is buffered, adjusted in amplitude, and used to drive a power amplifier which is short-circuit protected and provides the capability to driver loads as low as 50 ohms impedance.

Functional

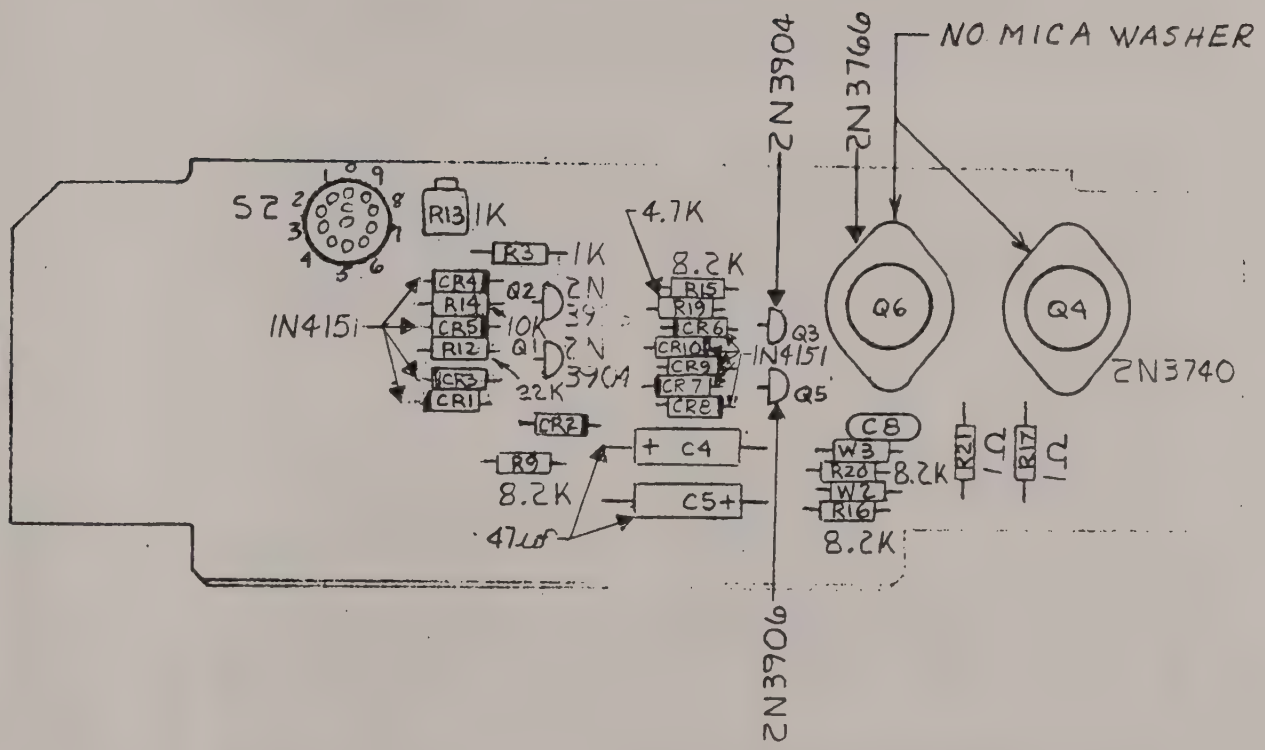
From one of nine bus lines the selector switch (or jumper wire -31 through -39) directs the input to a gate composed of R7, R8, R9, CR1, CR2, Q1 and R23. When the input which is equivalent to a DTL gate is logic level ZERO, Q1 is non-conductive (due to CR1), its collector and Q2 base and emitter are all at a dc voltage set by the dc level adjust. Q2 collector resistor, R19, biases Q5, Q6 to keep approximately zero volts at the output. When the input at the gate is logic level ONE, R9 passes current to Q1 base through the diodes so that Q1 turns on and its collector provides current drive to Q2 base, causing Q2 to turn on. Thus, Q2 collector becomes a + voltage (as determined by the setting of R13). The output of the amplifier at pin 19 becomes equal to the Q2 collector voltage. CR10 is a clamp to prevent negative drive to Q6.

The DC level adjust will provide output levels from 0.4 V to 15 volts (DC level adjust). CR4 and CR5 eliminate the dead band at the end of the potentiometer, R13.

When the collector of Q2 becomes positive, CR9 conducts current from R19 cutting off Q5 and allowing R15 to supply current to Q3, which drives the output stage Q4. In the case of a positive output being short circuited, the voltage across R17, R18 develops a voltage equal to that of CR6, CR8, and Q3, EB, thus bias at Q3 base isn't sufficient to drive Q4 and Q4 becomes limited. Therefore, the output at pin 19 is short-circuited protected.


REVISIONS
F CHG'D CB FROM .05 µF
G DWG NO. WAS 211603-7-30
C CR3 WAS IN4830; CR3 WAS JUMPER
D ADDED CB
E DELETED R7, R8, R10, R11.
+VCC
+16V
R15 8.2K
R16 8.2K
Q4 2N3740
Q3 2N3904
CR6 IN4151
CR7 IN4151
R17 1Ω 1/2 W
CR8 IN4151
R21 1Ω 1/2W
19
20
X
OUTPUT
CR9 IN4151
Q5 2N3906
Q6 2N3766
CR10 IN 4151
R19 4.7K
R20 8.2K
-VCC
-16V
C8 .047µF
S2 D.C. CHANNEL SELECT
F H J K L M N P R
1 2 3 4 5 6 7 8 9 0 C
+VCC
R9 8.2K
CR1 IN4151
CR2 IN4151
CR3 IN4151
R3 1K
Q1 2N3904
R12 22K
Q2 2N3906
R14 10K
R13 1K
D.C. LEVEL ADJ.
CR4 IN4151
CR5 IN4151
+16V
+VCC
GND
-VCC
-16V
23 44 W2
C4 47µF 20V
23 22 C5 47µF 20V
22 Z W3
-39 S2-C S2-9
-38 S2-C S2-8
-37 S2-C S2-7
-36 S2-C S2-6
-35 S2-C S2-5
-34 S2-C S2-4
-33 S2-C S2-3
-32 S2-C S2-2
-31 S2-C S2-1
FROM TO
JUMPER
-30 WITH 10 POS. SWITCH
-NO DESCRIPTION
NO SWITCH
LIST OF MATERIALS
DRAWN 12-19-67
CHECK
ENGR
MFGR 12/19/67
APPROVAL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCES
.X
.XX
.XXX
ANGLES ±
MATERIAL
DO NOT SCALE DRAWING
DWG SIZE C
SH 1 OF 1
AUSTRON INC AUSTIN, TEXAS
SCHEMATIC D.C. LINE DRIVER
DWG NO 12302603-30
REV G

A	REPLACED R23 & 24 WITH W2 & 3		443	1-5-72	PCH
B	DELETED R18, 22		445	2-20	JW
C	CR3 WAS W4		468	5-10	JW
C1	INTERCHANGE LOC OF CR7, CR8	-	-	5-14	
D	ADDED C8	-	11166	5-22	VID
E	DELETED R7, R8, R10, R11.	-	11671	5-23-73	JW
F	DWG WAS 21603-4-30		4837		
G	REVISED PER ECO 7032	-	-	12-6-73	



-39	S2-C	S2-9
-38	S2-C	S2-8
-37	S2-C	S2-7
-36	S2-C	S2-6
-35	S2-C	S2-5
-34	S2-C	S2-4
-33	S2-C	S2-3
-32	S2-C	S2-2
-31	S2-C	S2-1
	FROM JUMPER	TO
-30	10 POS. SW.	
-29	DESCRIPTION	

6-34

AUSTRON INC
AUSTIN, TEXAS

ASSEMBLY
P.C. BOARD
DC LINE DRIVER

ASSEMBLY PCB ASSY,D.C. LINE DRIVER
ASSEMBLY NUMBER 10302603-31
REFERENCE DESIGNATOR PREFIX 1A
QUANTITY 1 EA

REF DES	PART DESCRIPTION	AUSTRON PART	MFG PART	FIC
C4	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C5	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
C8	47 UF 20V 20 CAP TANT	608116-0477	196D476X0020PE	56289
CR1	50V DIO SIG	7011N4151	1N4151	13715
CR2	50V DIO SIG	7011N4151	1N4151	13715
CR3	50V DIO SIG	7011N4151	1N4151	13715
CR4	50V DIO SIG	7011N4151	1N4151	13715
CR5	50V DIO SIG	7011N4151	1N4151	13715
CR6	50V DIO SIG	7011N4151	1N4151	13715
CR7	50V DIO SIG	7011N4151	1N4151	13715
CR8	50V DIO SIG	7011N4151	1N4151	13715
CR9	50V DIO SIG	7011N4151	1N4151	13715
CR10	50V DIO SIG	7011N4151	1N4151	13715
MP1	CARD EJECTOR	506020-2030	S203	18677
MP2	CARD EJECTOR	506020-2030	S203	18677
Q1	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q2	0.31W TO-92 XSTR PNPS SH	7022N3906	2N3906	81349
Q3	0.31W TO-92 XSTR NPNS SH	7022N3904	2N3904	81349
Q4	25 W XSTR PNPS	7022N3740	2N3740	04713
Q5	0.31W TO-92 XSTR PNPS SH	7022N3906	2N3906	81349
Q6	20W TO-66 XSTR NPNS	7022N3766	2N3766	04713
R3	RES FXD COMP 1 K 1/4W 05%	651100-0102	RC07GF102J	81349
R9	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R12	RES FXD COMP 22 K 1/4W 05%	651100-0223	RC07GF223J	81349
R13	1K 1W 5 POT PCENPC22T	659042-0102	224P-1-102	73138
R14	RES FXD COMP 1 K 1/4W 05%	651100-0102	RC07GF102J	81349
R15	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R16	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R17	RES FXD COMP 1 OHM 1/2W 05%	651101-01R0	RC20GF1R0J	81349
R19	RES FXD COMP 4.7 K 1/4W 05%	651100-0472	RC07GF472J	81349
R20	RES FXD COMP 8.2 K 1/4W 05%	651100-0822	RC07GF822J	81349
R21	RES FXD COMP 1 OHM 1/2W 05%	651101-01R0	RC20GF1R0J	81349
W2	JUMPER 22AWG INSULATED	520440-2007	L-2007-1	55210

7. SPECIAL MODIFICATIONS

7.1. SCOPE OF SECTION

Section Seven provides circuit descriptions, logic and schematic diagrams, assembly drawings, and parts lists for any special or non-standard options included in your Model 8120.

7.2. MODIFICATIONS INCLUDED

Modifications to the Model 8120 requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.

No special modifications are included in the Model 8120.

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MP MASTER
MA31211